

Compal Confidential

Kabylake-U M/B Schematics Document

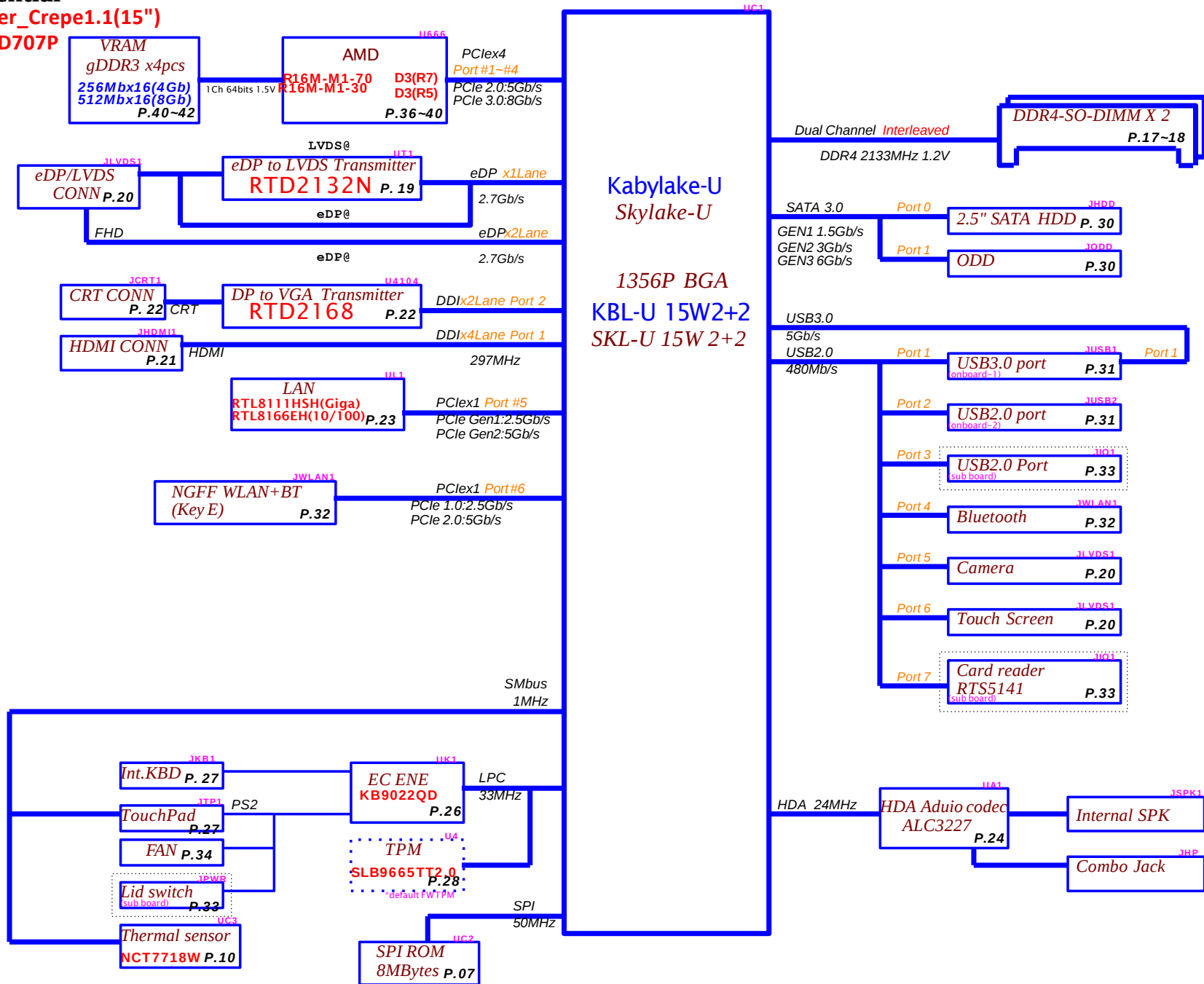
Intel ULV Processor with DDR4 SODIMMx2

Date : 2016/05/11

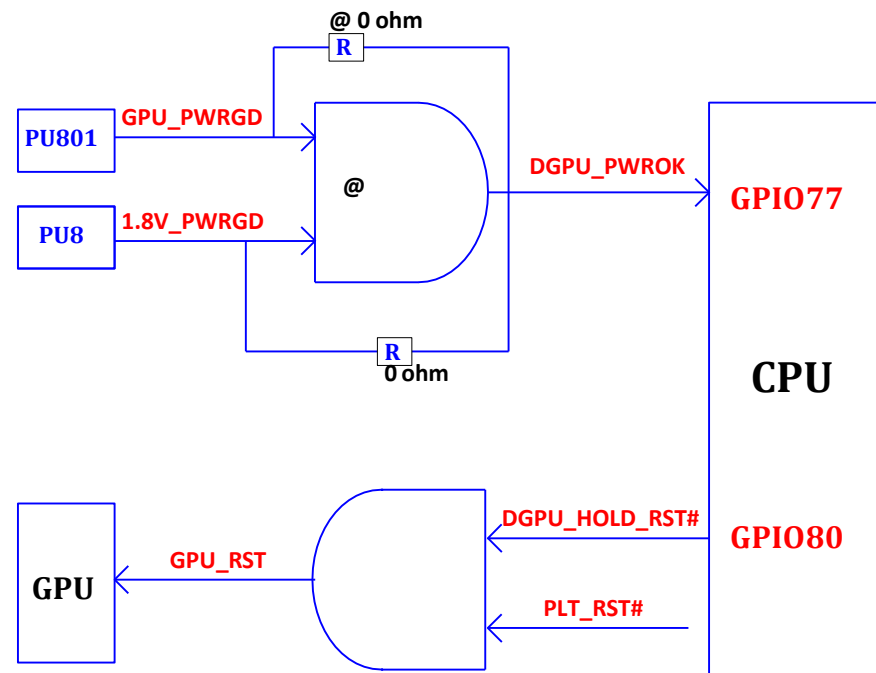
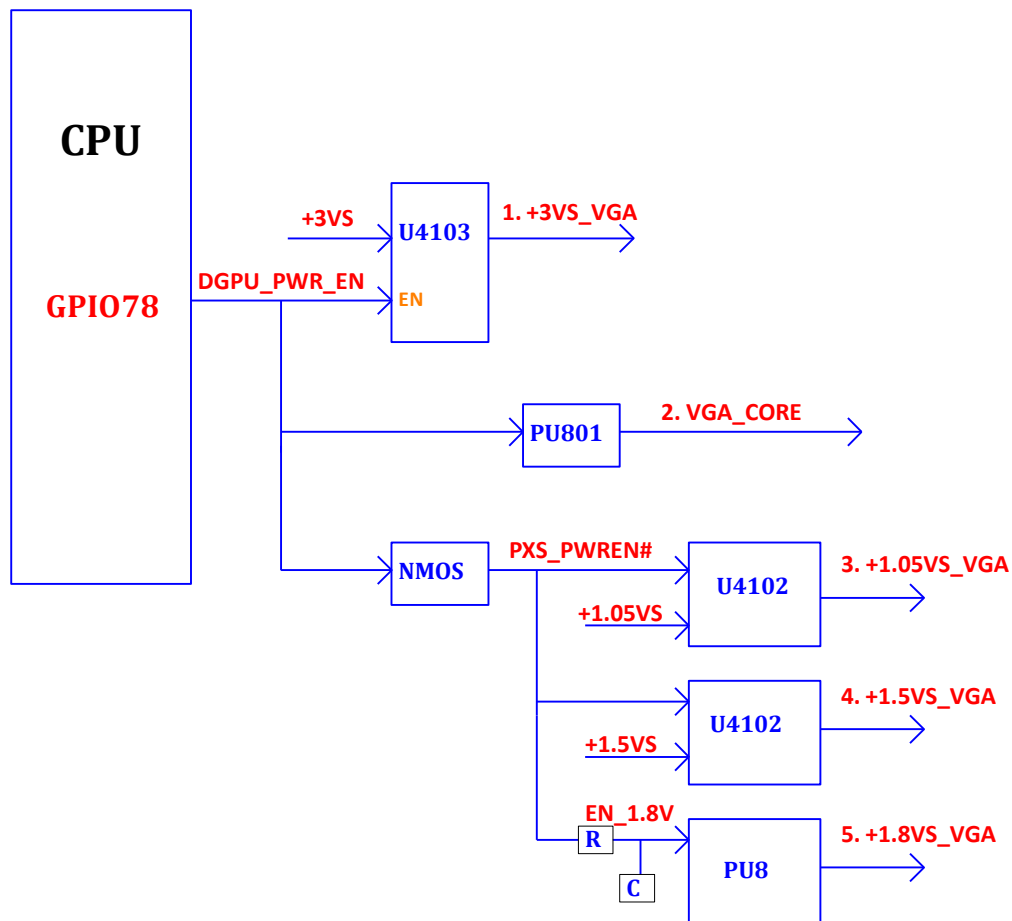
Version : 4.0

Project : *Diner_Crepe1.1(15")*
BDL50 : LA-D704P

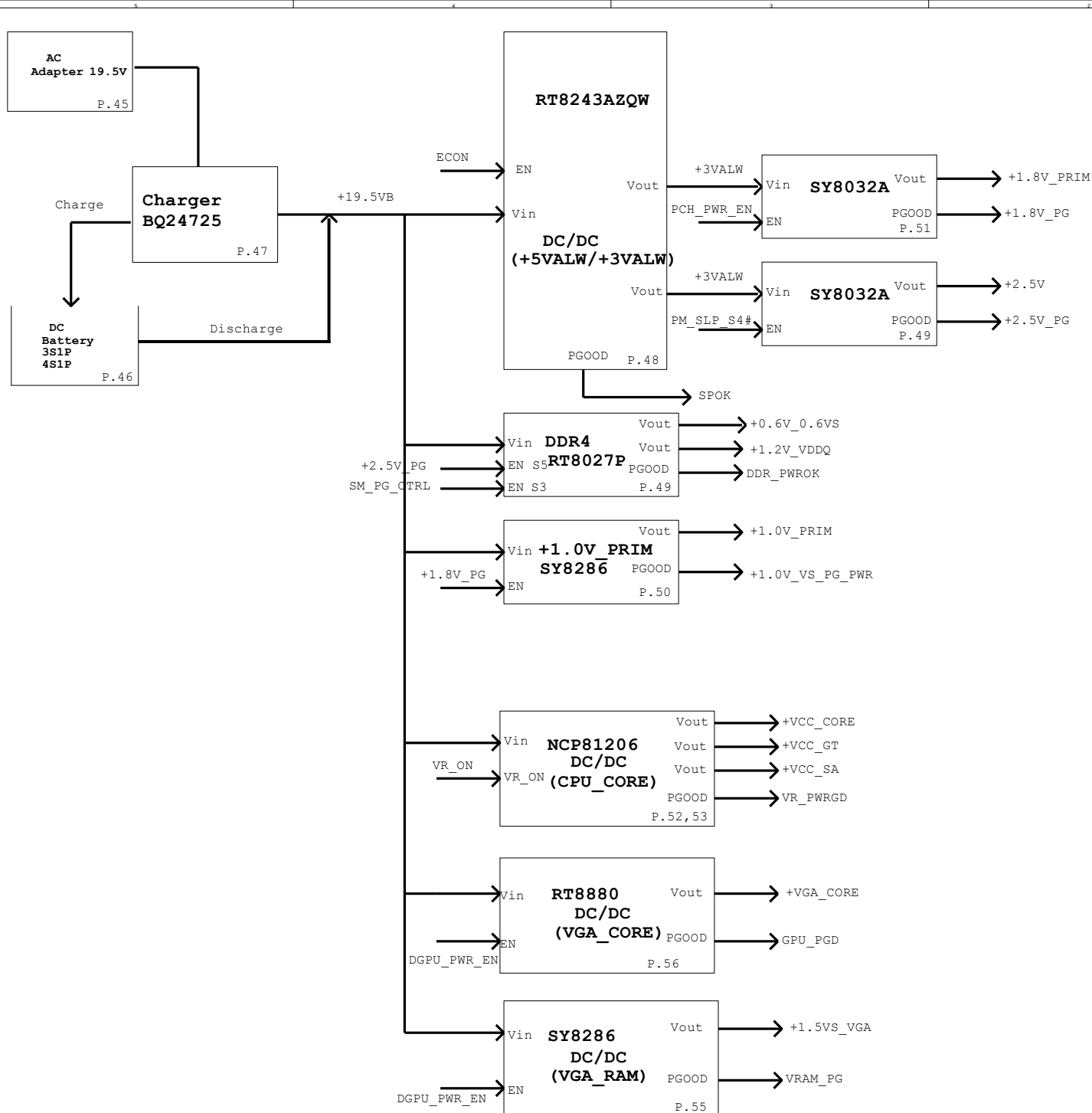
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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	
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				Site Document Number	Rev
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				Date	Wednesday, May 11, 2016
				Sheet	1 of 60



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title Block Diagrams	
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Revised Date	Designed Date	RSVD
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Version: 1.0		0.1



CPU DC/DC		52-5
NCP81206		
INPUTS	OUTPUTS	
B+	VCC_SA VCC_GT VCC_VORE	
SYSTEM DC/DC		
RT8243AZQW		
INPUTS	OUTPUTS	
B+	+5VALW/+3VALW	
SYSTEM DC/DC		
RT8207P / 8032		
INPUTS	OUTPUTS	
B+	+1.2V_VDDQ +0.6V_0.6_VS	+2.5V
SYSTEM DC/DC		
SY8286		
INPUTS	OUTPUTS	
B+	+1.0V_PRIM	
SYSTEM DC/DC		
SY8032A		
INPUTS	OUTPUTS	
+3VALW	+1.8V_PRI	
SYSTEM DC/DC		
RT8880		
INPUTS	OUTPUTS	56-1
B+	+VGA_CORE	
SYSTEM DC/DC		
SY8286		
INPUTS	OUTPUTS	5
B+	+1.5VS_VGA	

Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.2V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.6VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

BOM Structure Table (1/2)

Function	Stuff	Un-Stuff
DGPU SKU	PX@	
UMA SKU	UMA@	
SPI_I03(MOW36)	ES@	
Crystal (DIS)	XTALPX@	
Crystal	XTAL@	
Green CLK(UMA)	GCLX@	
Green CLK(DIS)	GCLKPx@	
TPM	TPM@	

SOC SMBUS Address Table (TBC)

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SMBCLK SMBDATA	+3VS	DIMM1	TBC	TBC	0xA2
		Touch PAD	TBC	TBC	TBC
SMLOCLK SML0DATA	+3VS	ME FW	0x48/0x49	TBC	0x90/0x92
SML1CLK SML1DATA	+3VS	EC	TBC	TBC	TBC
		DGPU	TBC	TBC	TBC
		PCH	TBC	TBC	TBC

EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
SMBUS Port 1	+3VL_EC	BAT	0x16
		CHGR	0x12
SMBUS Port 2	+3VS	dGPU	TBC
		Thermal Sensor	0x4C
		PCH	TBC

Power State

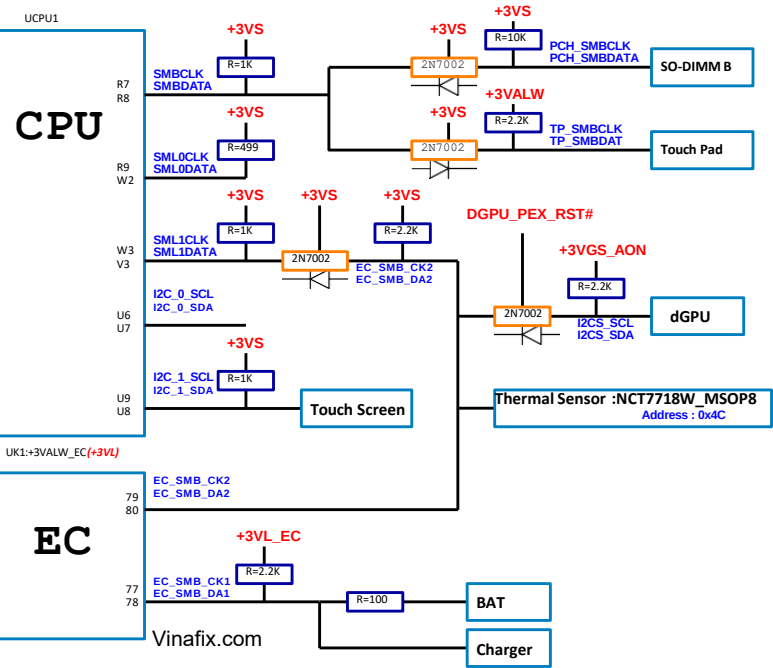
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

<USB2.0 port>

USB2.0 port	DESTINATION	
	UMA	Dis
1	USB 2.0/3.0	USB 2.0/3.0
2	USB 2.0/3.0	USB 2.0/3.0
3	USB 2.0 OFF BOARD	USB 2.0 OFF BOARD
4	WLAN	WLAN
5	Camera	Camera
6	TOUCH SCREEN	TOUCH SCREEN
7	CR	CR
8		
9		
10		

<PCI-E,SATA,USB3.0/CLK>

Lane#	PCI-E	SATA	USB3.0	DESTINATION		CLK
				UMA	Dis	
1			1	USB3.0	USB3.0	X
2			2	USB3.0	USB3.0	X
3			3	USB3.0(Charger)	USB3.0(Charger)	X
4			4	USB3.0(IO Board)	USB3.0(IO Board)	X
5	1		5	X	GPU(DIS only)	CLK0
6	2		6	X	GPU(DIS only)	
7	3			X	GPU(DIS only)	
8	4			X	GPU(DIS only)	
9	5			LAN	LAN	CLK1
10	6			WLAN	WLAN	CLK2
11	7	0		2.5"HDD	2.5"HDD	X
12	8	1		ODD	ODD	X
13	9			Card reader(PCI-E)	Card reader(PCI-E)	CLK3
14	10			X	X	X
15	11	1*		X	X	X
16	12	2				X



Load BOM Option Table

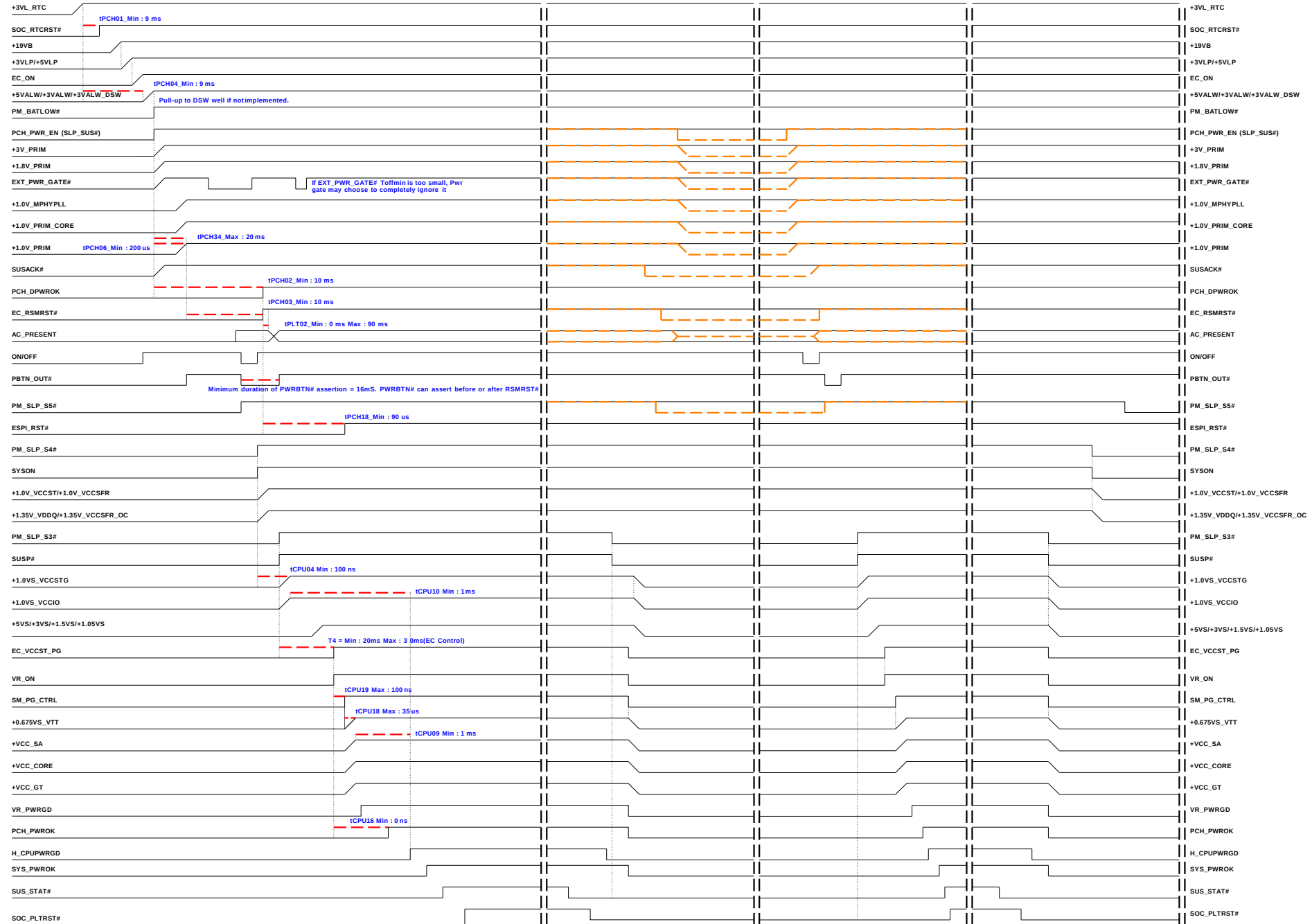
BOM Number	Load BOM Option
4519YN32L01(UMA)	
4519YN32L02(DIS)	

G3->S0

S0->S3/DS3

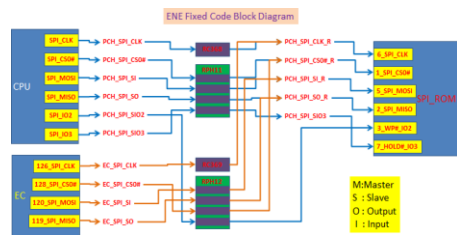
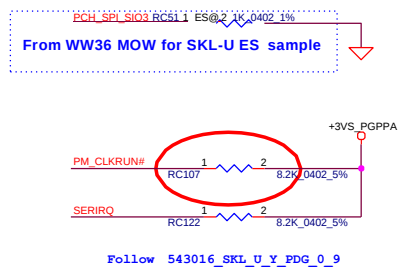
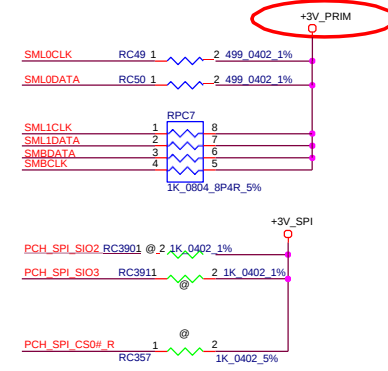
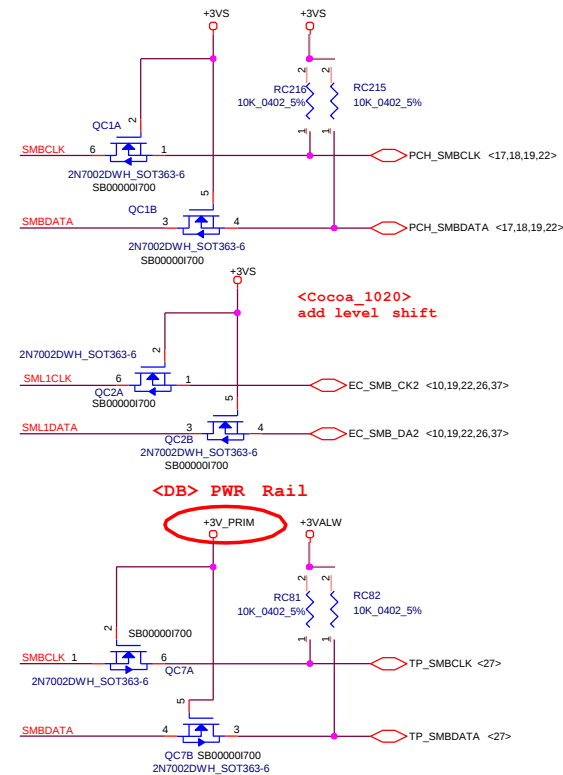
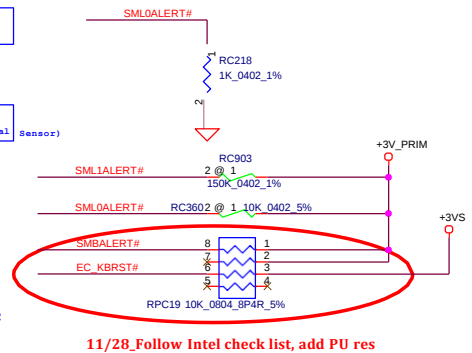
S0/DS3->S0

S0->S5

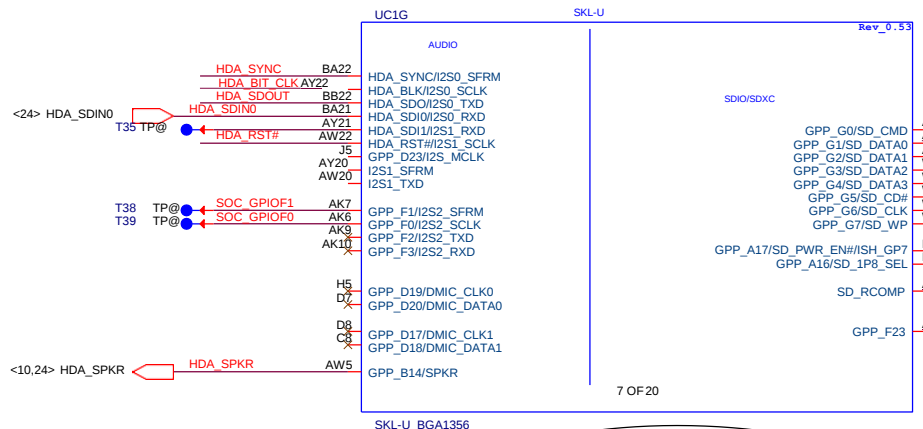




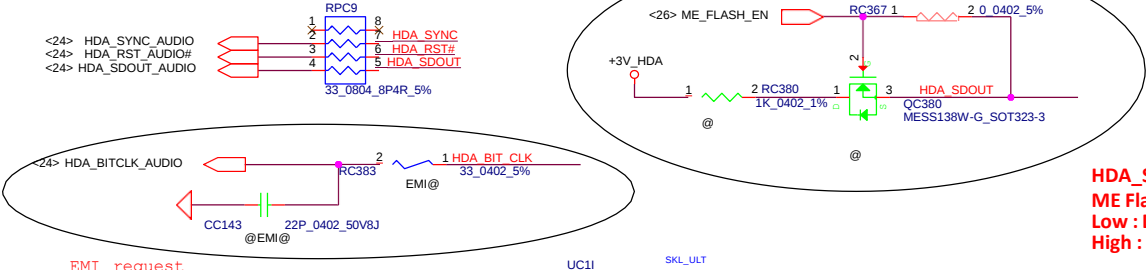
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Issued Date	2014/05/19	Deciphered Date	2015/12/31	Title SKL-U(1/12)DDIMSIC.XDP.EDP	Rev v0.
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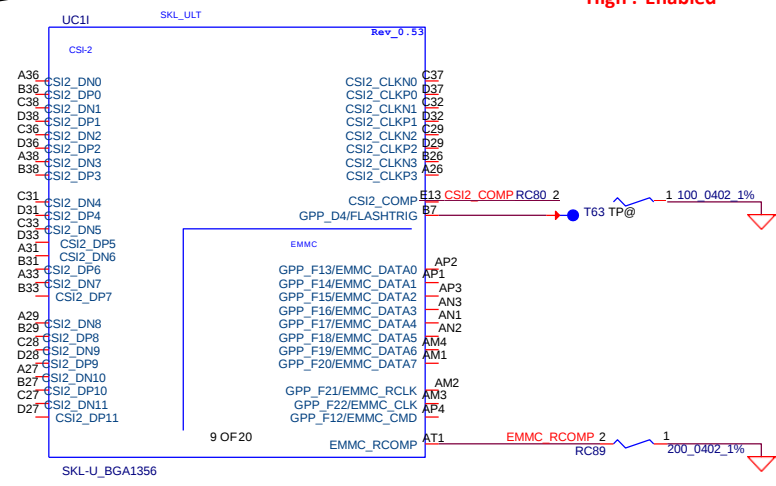
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Issued Date	2014/12/11	Deciphered Date	2015/12/31	Title	
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HDA for AUDIO

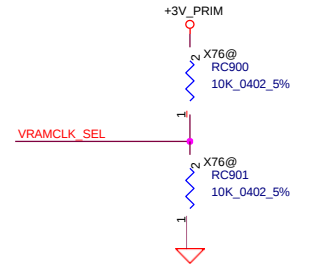


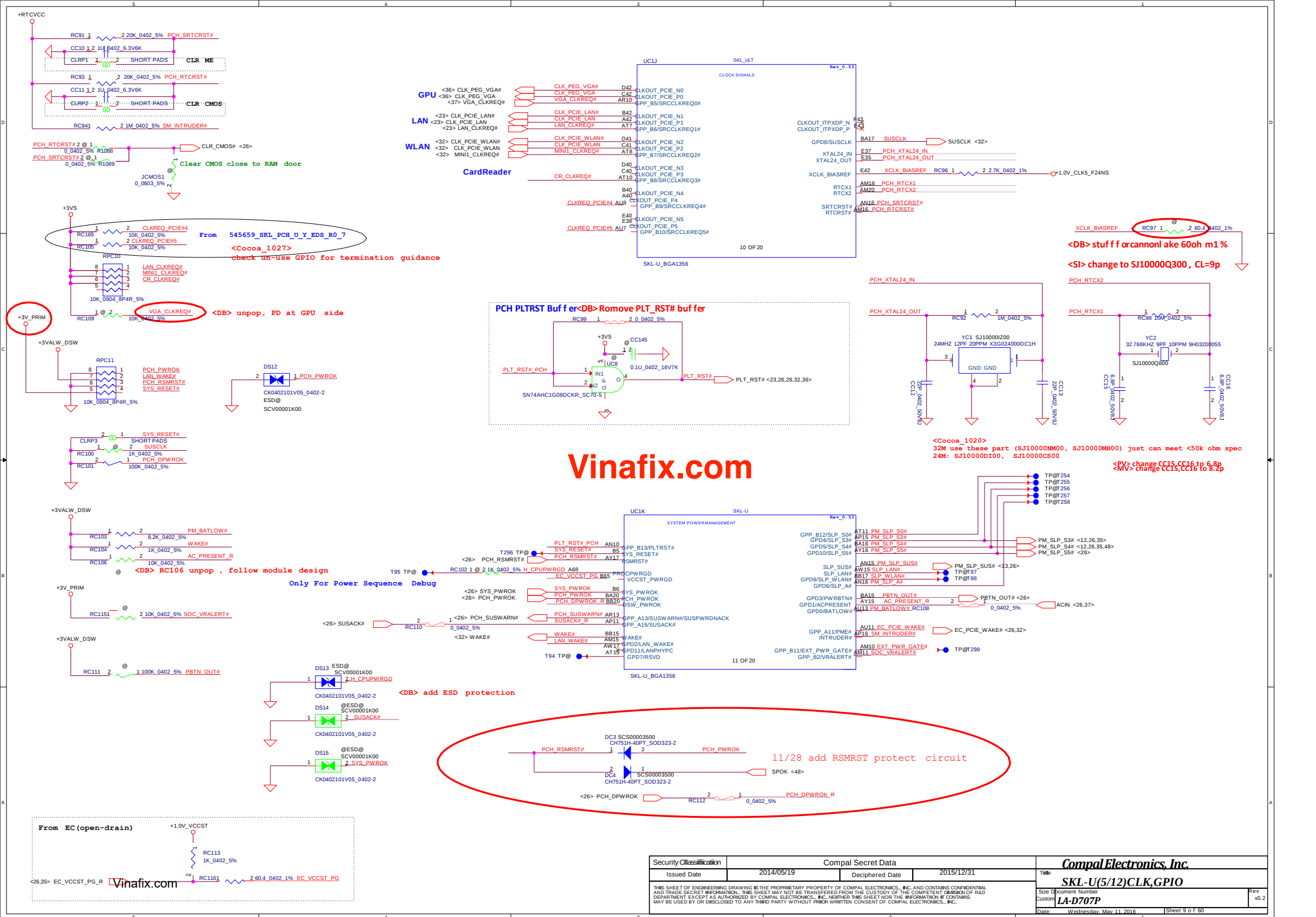
HDA_SDOUT:
ME Flash Descriptor Security Override
Low : Disabled(Default)
High : Enabled



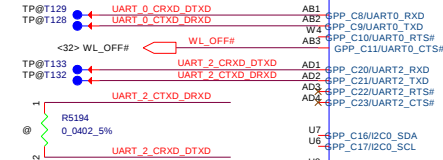
PROJECT_ID	UMA	DIS
	0	1

VRAM Clock	900MHz	1000MHz
	0	1





<DB> add TP by BIOS



Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.--> AAX05 Use

1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

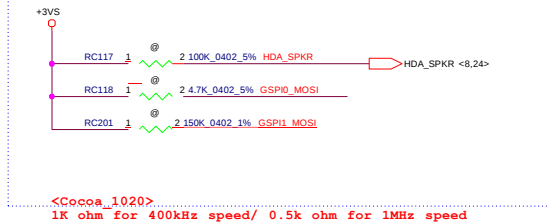
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

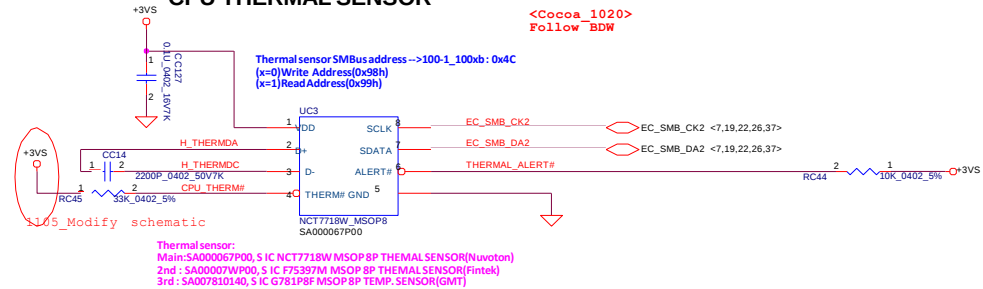
0 = SPI Mode --> AAX05 Use

1 = LPC Mode

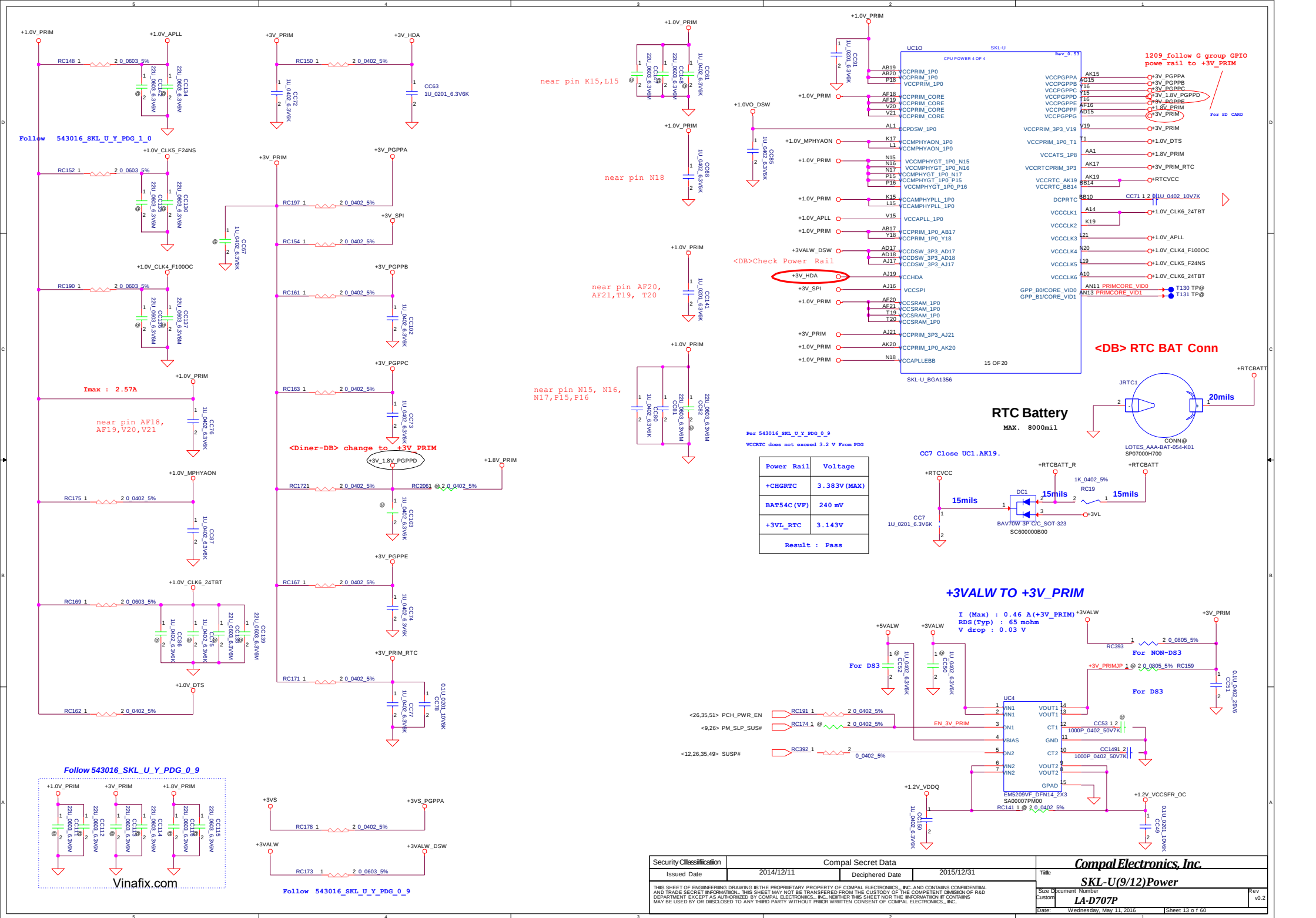
Strap Pin

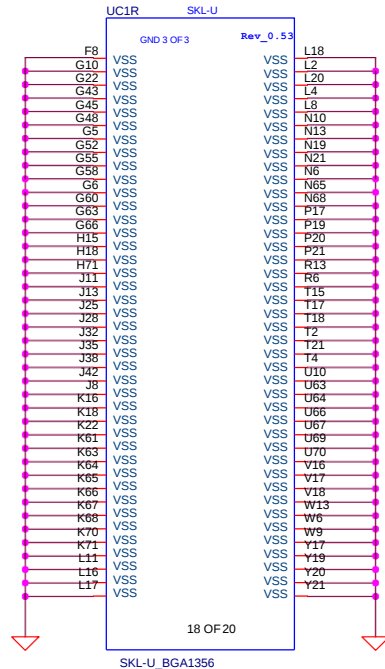
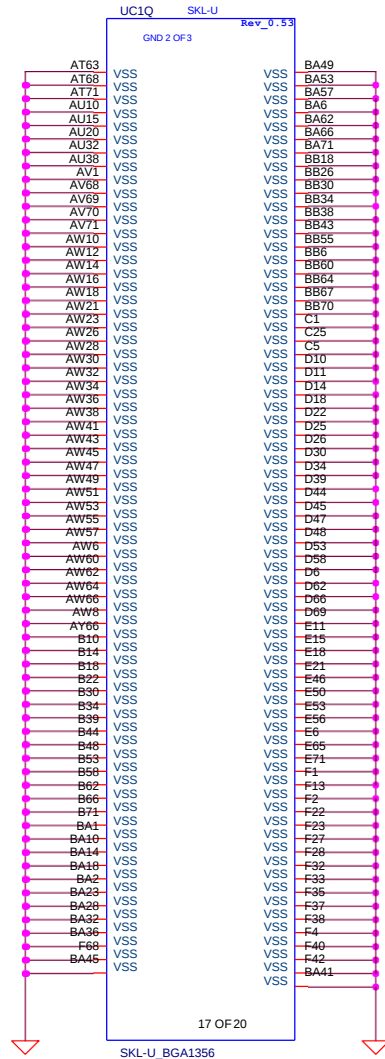
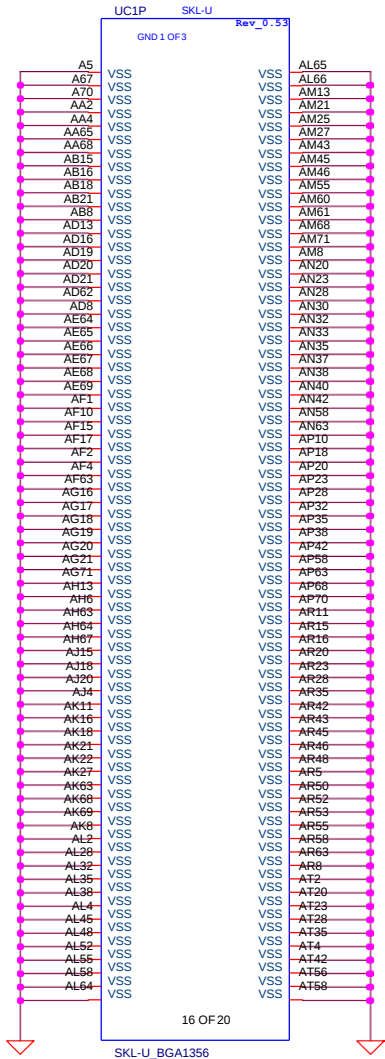


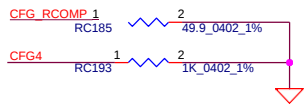
CPU THERMAL SENSOR



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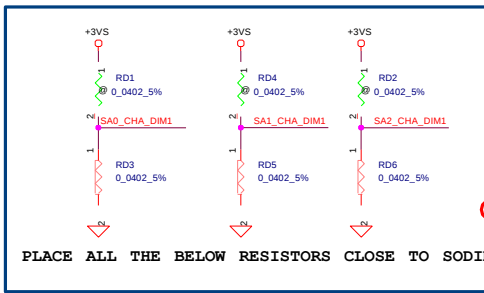
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CHANNEL-A

REVERSE TYPE (5.2 mm)

Interleaved Memory

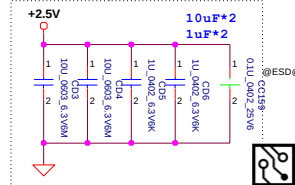
TOP: JDIMM1 CONN Non-ECC DIMM



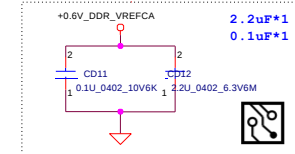
SPD ADDRESS FOR CHANNEL A :
 WRITE ADDRESS: 0XA0
 READ ADDRESS: 0XA1
 SA0 = 0; SA1 = 0; SA2 = 0.
 DDR4 POR OPERATING SPEED: 1867 MT/S
 STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM1.257,259

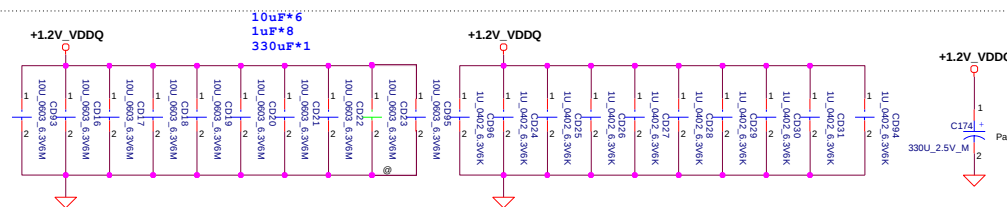
Layout Note:
Place near JDIMM1.258



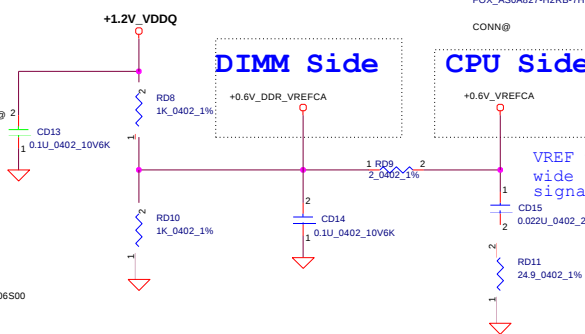
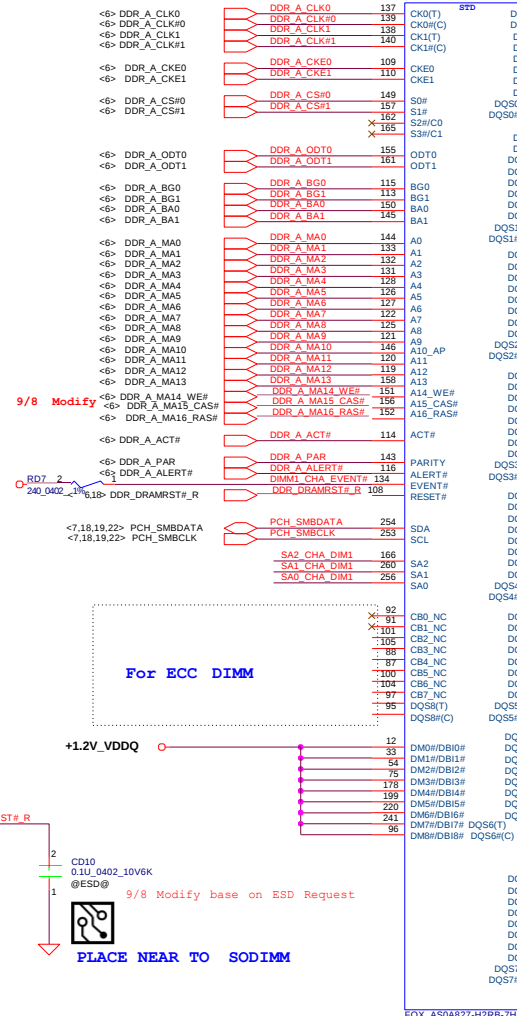
Layout Note:
PLACE THE CAP near JDIMM1. 164



Layout Note:
Place near JDIMM1



Part Number: LTX0069GA0
 Part Value: S SOCKET FOX AS0A827-H2RB-7H 260P DDR4



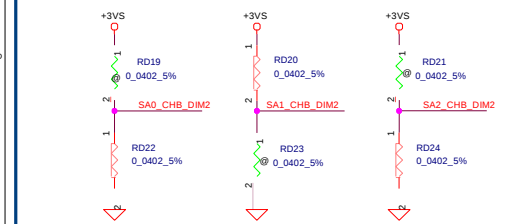
VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

CHANNEL-B

Interleaved Memory

STD (5.2 mm)

TOP: JDIMM2 CONN Non-ECC DIMM

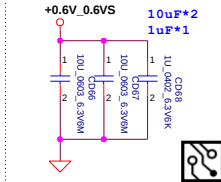
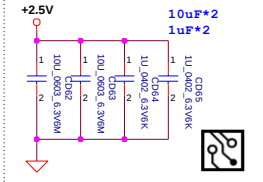


PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

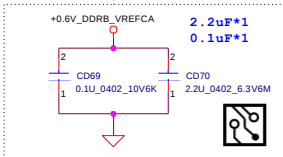
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM2.257,259

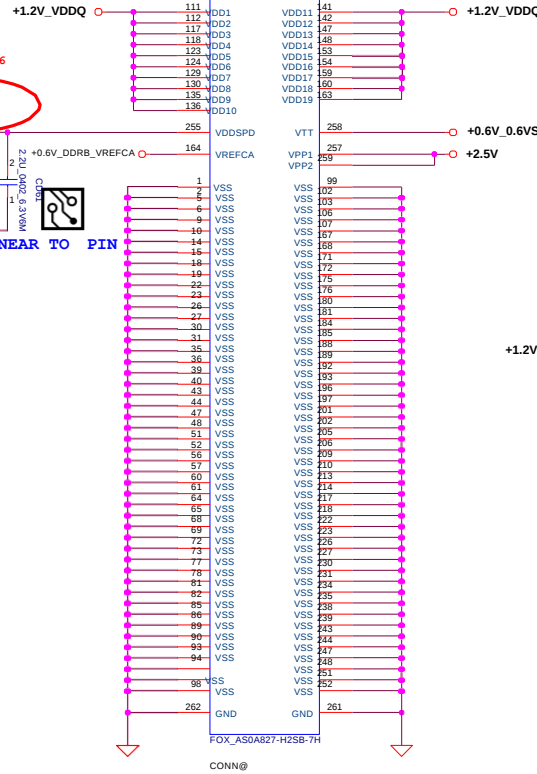
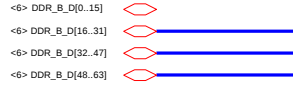
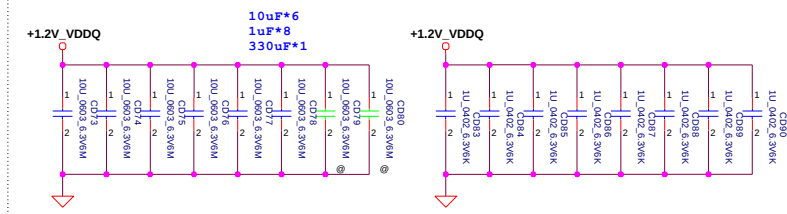
Layout Note:
Place near JDIMM2.258



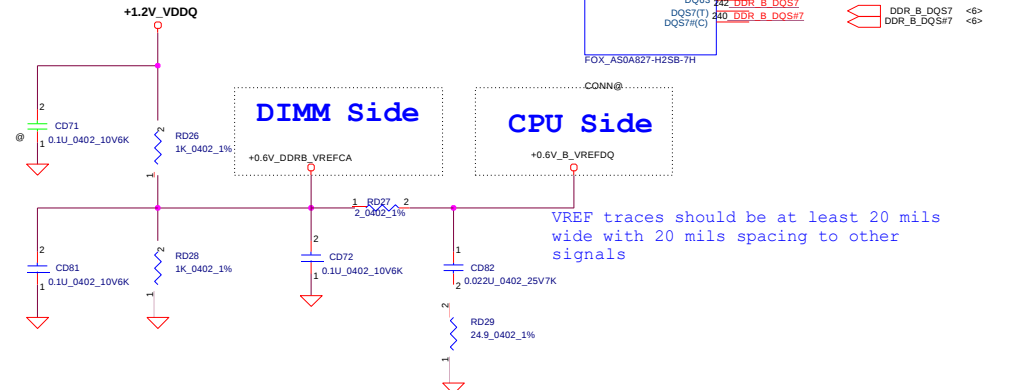
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2



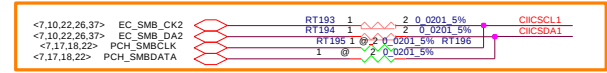
Layout Note:
Place near JDIMM2



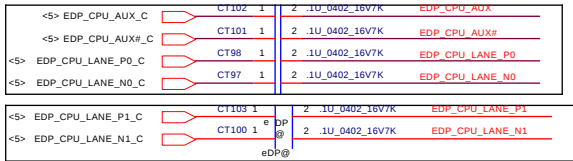
Part Number: LTCX0069FA0
Part Value: S SOCKET FOX AS0A827-H2SB-7H 260P DDR4



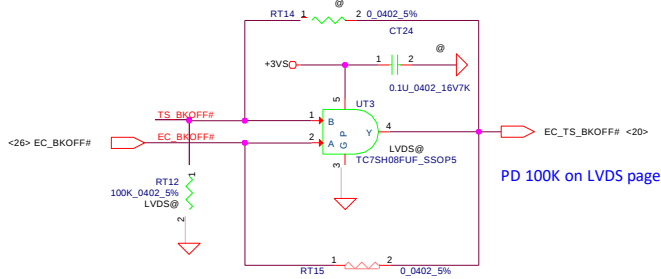
VREF traces should be at least 20 mils wide with 20 mils spacing to other signals



Layout notes
CC97~CC102 must closed to connector



DB phase :
add eDP Lan1 for FHD
20141117



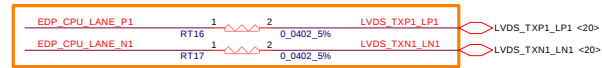
PD 100K on LVDS page

<LVDS Panel>

<CPU by PASS eDP>



Layout notes
RP6 RP9 RP10 must closed to connector



DB phase :
add eDP Lan1 for FHD
20141117

Layout notes
RT16~RT19 must closed to connector

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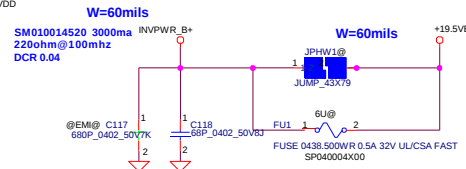
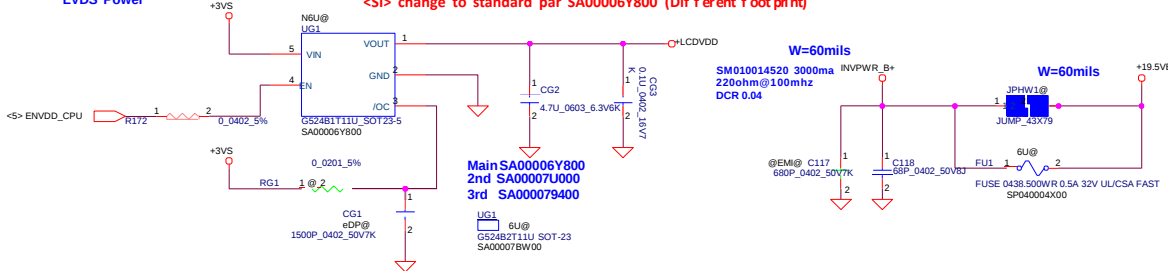
LVDS Power

<SI> change to standard par SA00006Y800 (Different footprint)

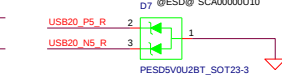
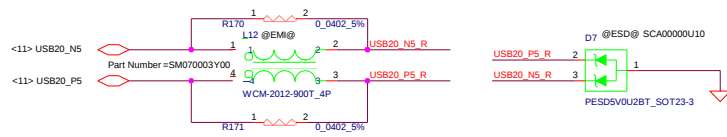
<5,6,7,9,10,11,13,17,18,19,21,22,23,24,26,28,32,33,34,35,36,37,38,52,55,56> +3VS

<38,47,48,49,50,53,55,56> +19.5VB

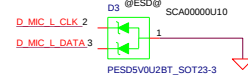
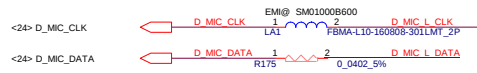
<7,13,23,26,27,30,33,35,48,49,50,51,55> +3VALW



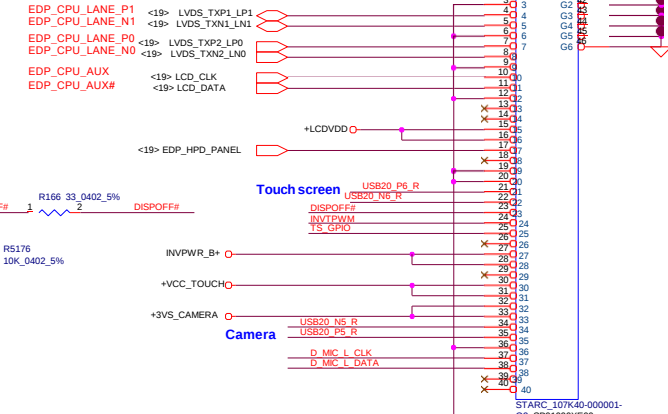
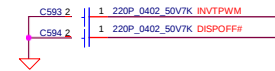
Camera



<DB>LA1/LA2 closed to Audio codec



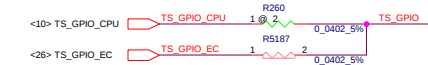
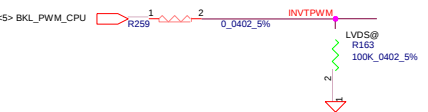
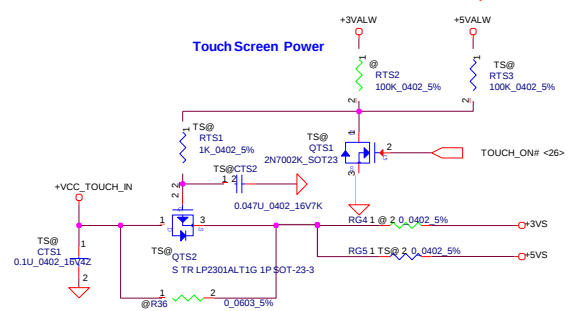
LCD/LED PANEL Conn.



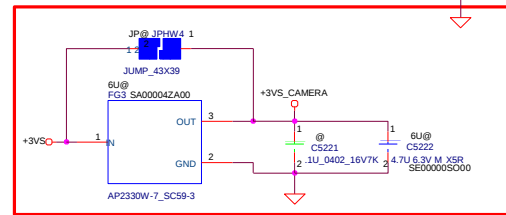
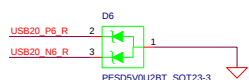
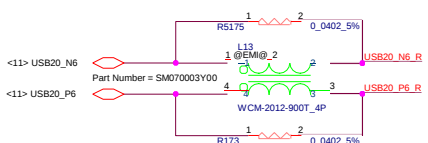
Touch Screen

<DB> for 5V/3V TS option

Touch Screen Power



<PV> Touch GPIO control by EC

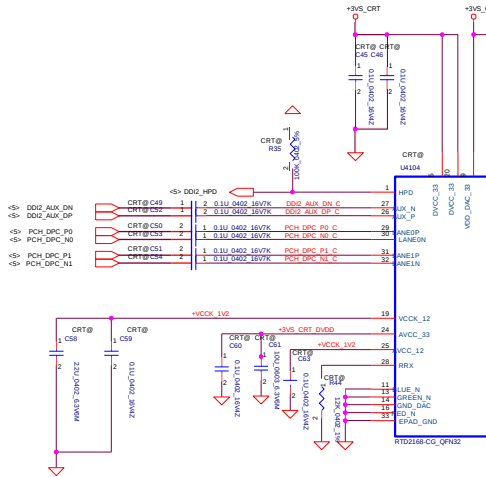
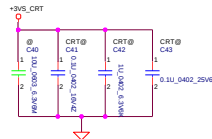
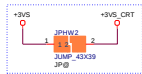


Vinafix.com

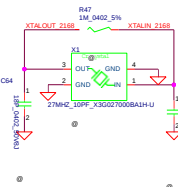
Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date
Deciphered Date	2015/07/08	Size Document Number
Size Document Number	LA-C707P	Rev
Rev	v0.2	Sheet 20 of 60
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DP to CRT converter

For Power consumption Measurement



Part Number = S400077U00



Embedded LDO

Select VCCK_V12 source from external 1.2V or embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

Mode Configure Table(Power On Latch)

	POL1_SDA(PIN22)	
	0	1
POL2_SCL(PIN23)	0	X
	1	ROM ONLY MODE
		EEPROM MODE

RTD2168 Supports three operation mode for system design.
Reserve 4.7K resistor pull high/low for mode selection

ROM ONLY Mode : PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high

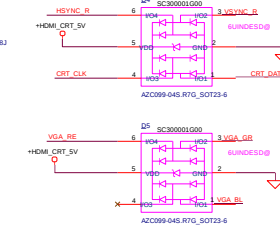
<0,21,24,26,27,30,34,35,53,56> +5V5
<5,6,7,9,10,11,13,17,18,19,20,21,23,24,26,28,32,33,34,35,36,37,38,52,55,56> +5V5
<21> +HDMI_CRT_SV

2014-11-24
Follow vendor suggest change 36 ohm



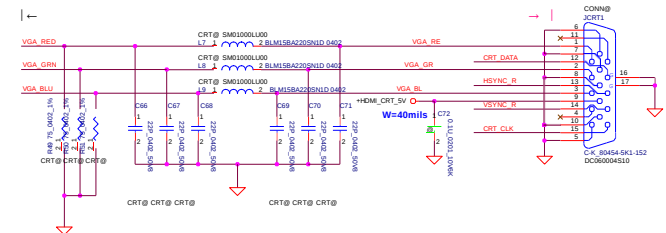
Layout notes
R61,R62,R58,R59 close to RTD2168
R55,R57,R60,R56 close to CONN

<KBL Sd> Change ESD diode package
D4&D5 Only Pop for 6U SKU India Country

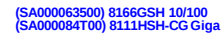


50 impedance

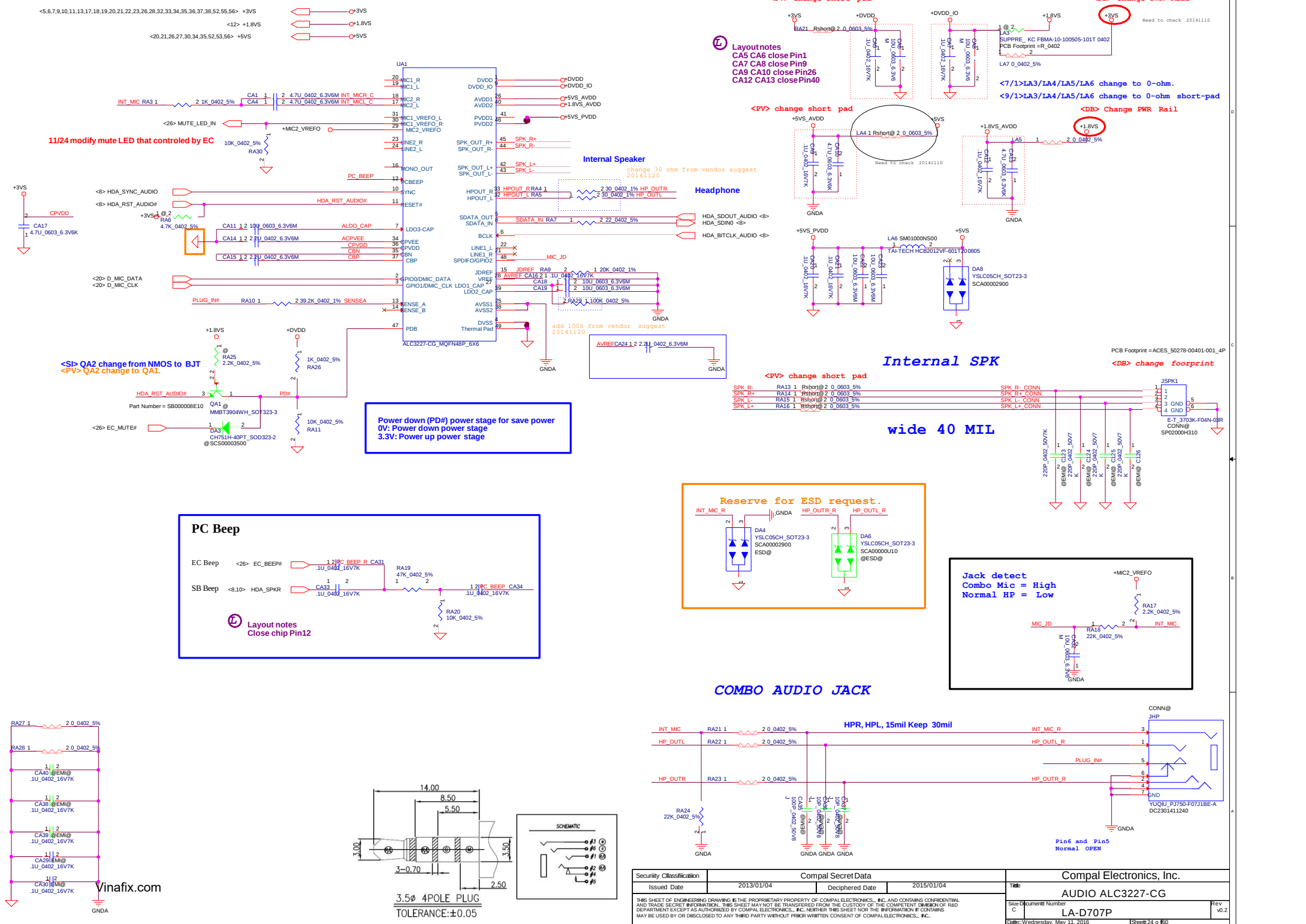
CRT Connector



Security Classification		Compall Secret Data		Compall Electronics, Inc.	
Revised Date	2014/02/19	Designed Date	2015/02/20	DP to CRT RTD2168	
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COMPALL ELECTRONICS, INC.				Rev	V0.1



CR RTS5237S move to S/B



<5,6,7,9,10,11,13,17,18,19,20,21,22,23,26,32,33,34,35,36,37,38,52,55,56> +3VS

<12> +1.8VS

<20,21,26,27,30,34,35,52,53,56> +5VS

11/24 modify mute LED that controlled by EC

PC BEEP

Internal Speaker

Headphone

Internal SPK

COMBO AUDIO JACK

PC BEEP

Jack detect

COMBO Mic = High

Normal HP = Low

Pin6 and Pin5

Normal OPEN

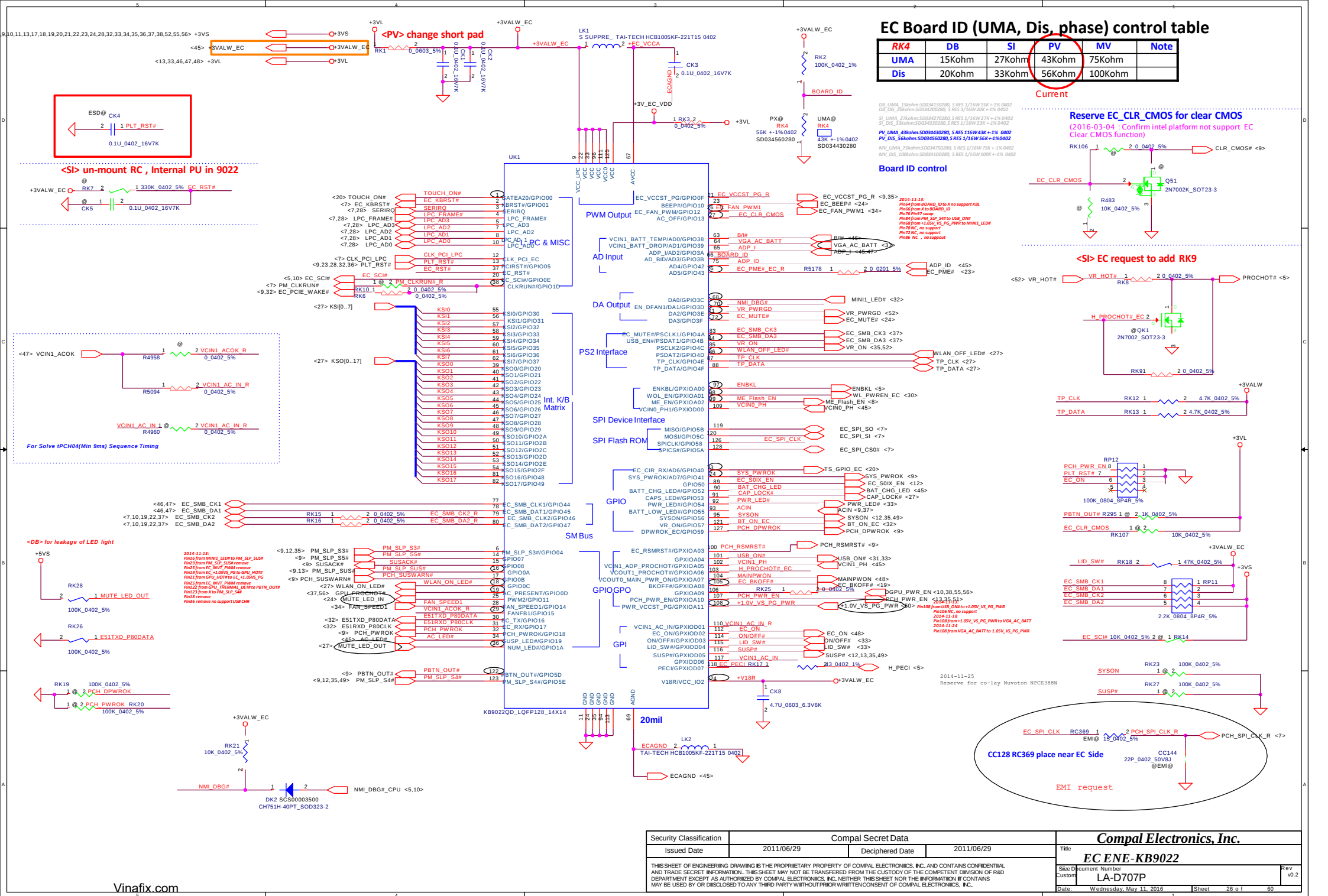
Vinafx.com

LA-D707P

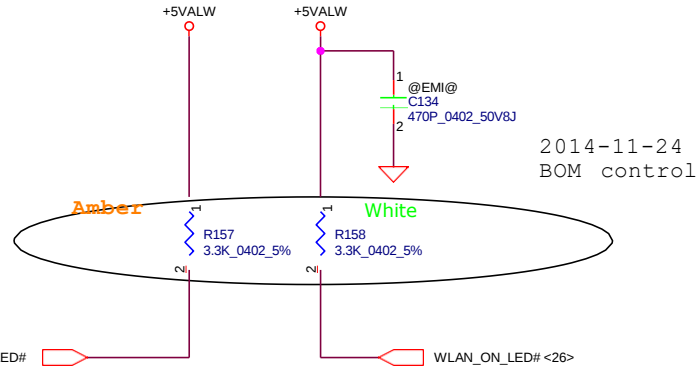
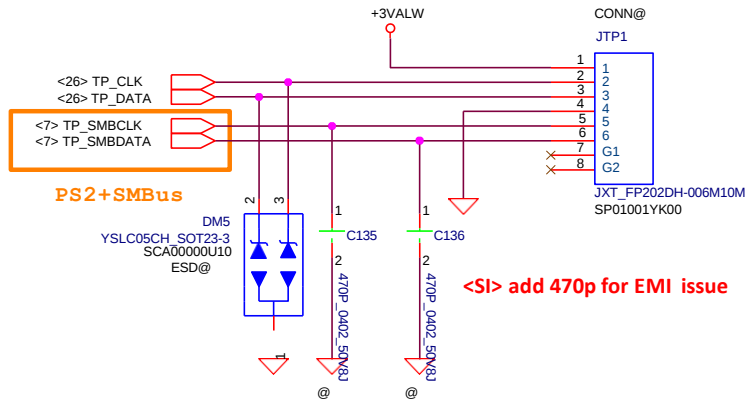
Rev v0.2

Wednesday, May 11, 2016

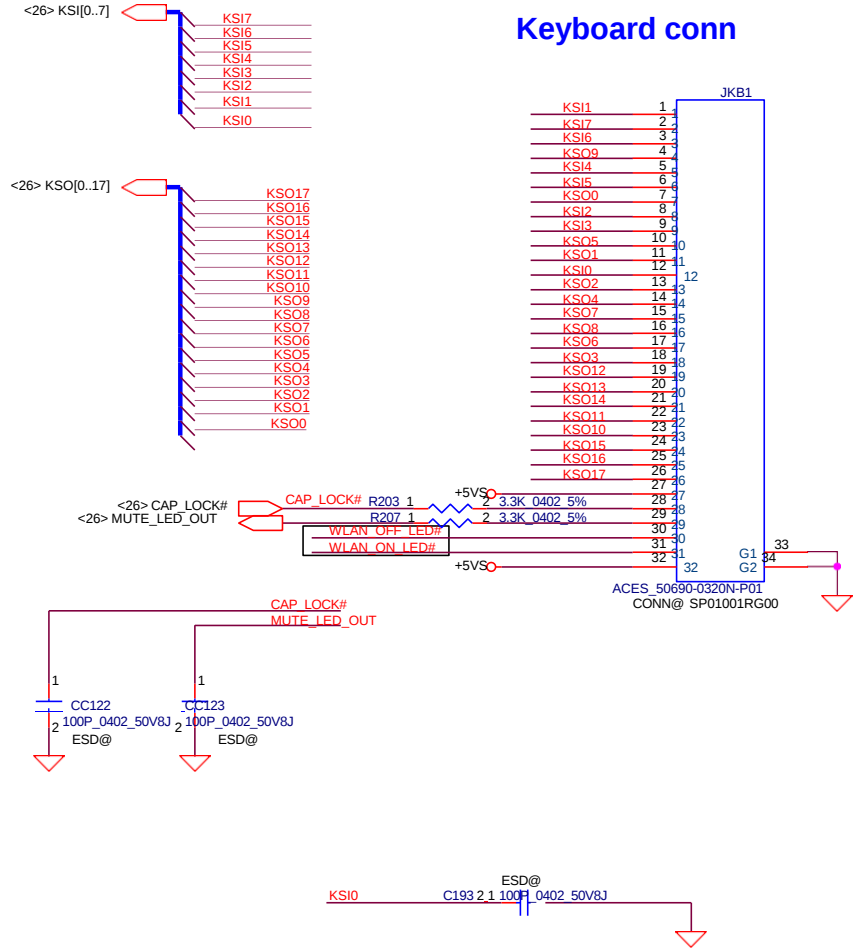
Sheet 24 of 80



TP Button BD Connector

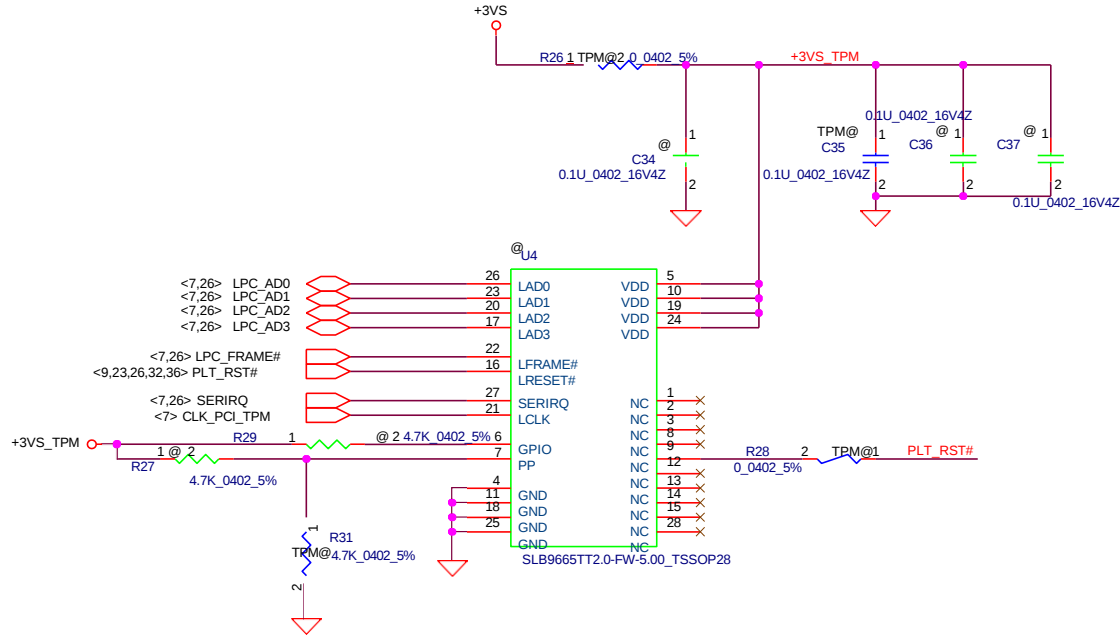


Keyboard conn



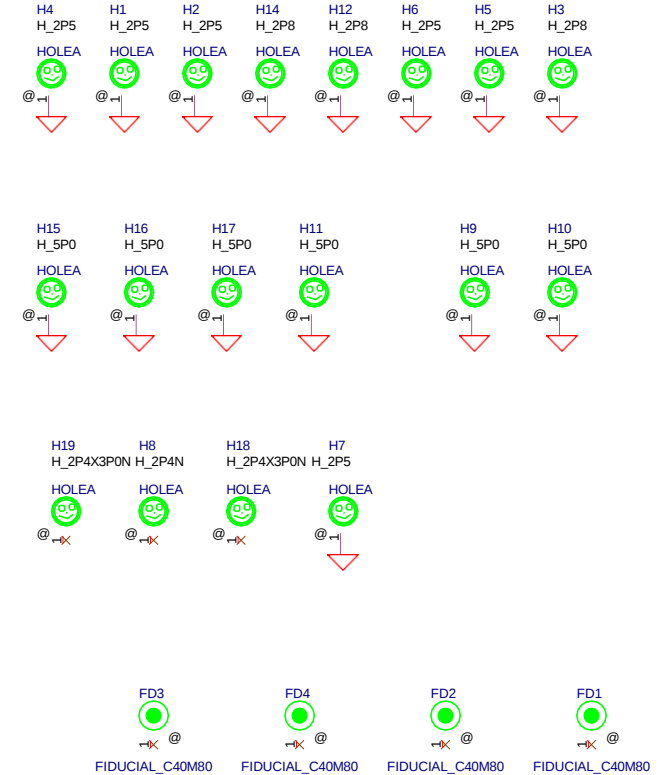
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	
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				Size Document Number	Rev
				B LA-D707P	v0.2
				Date: Wednesday, May 11, 2016	Sheet 27 of 60

TPM2.0



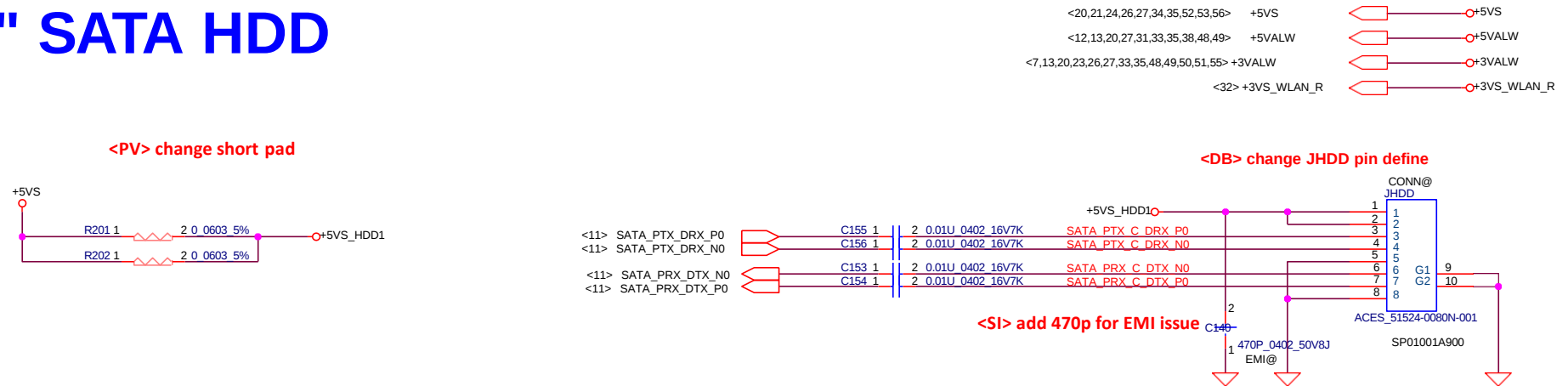
SLB9665 (SA00007XU00)-->TPM2.0
SLB9660 (SA00007AB00) -->TPM1.2

Screw Hole

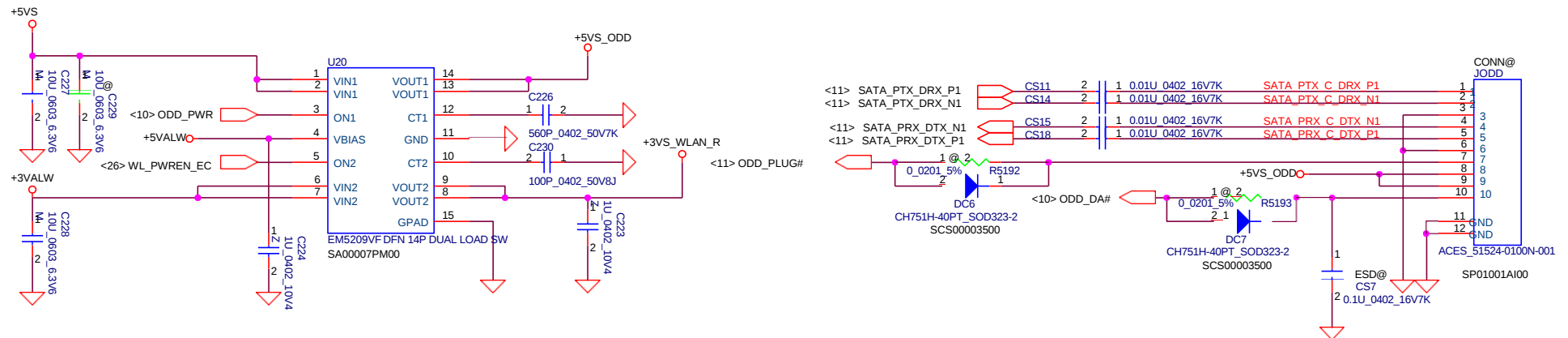


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	
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				Size Document Number	Rev
				LA-D707P	v0.2
				Date: Wednesday, May 11, 2016	Sheet 28 of 60

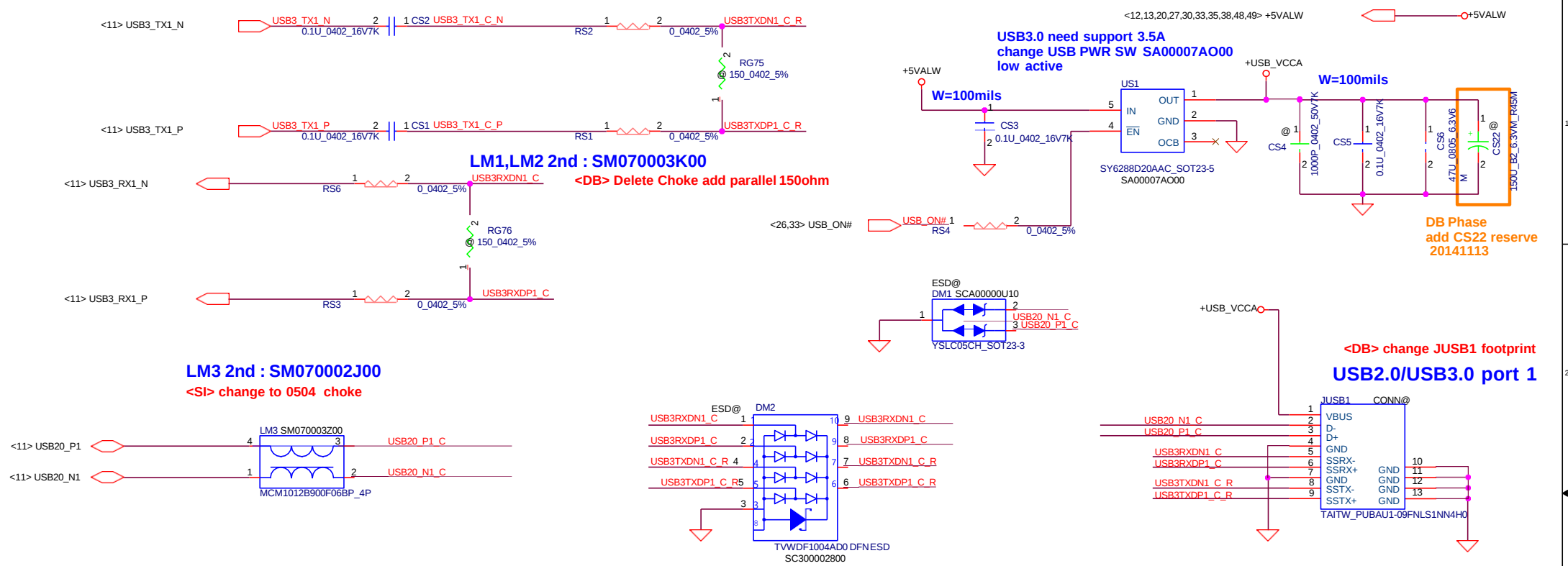
2.5" SATA HDD



2.5" SATA ODD

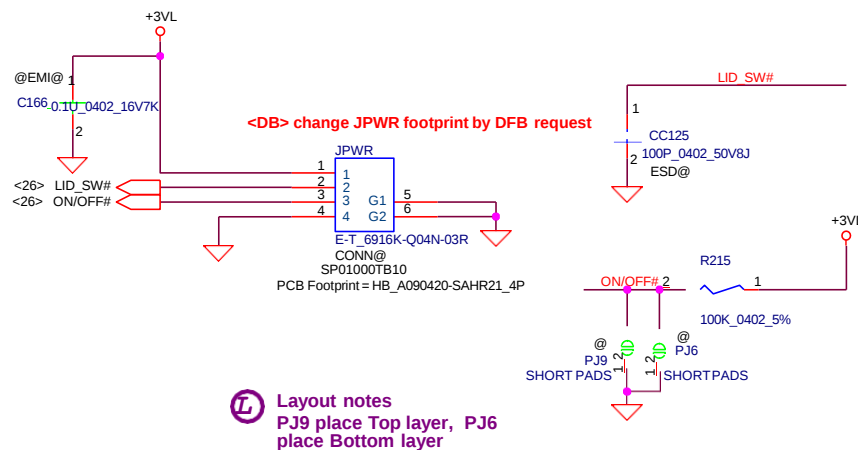


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	HDD/ODD Conn	
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				LA-D707P		
				Date: Wednesday, May 11, 2016	Sheet 30 of 60	

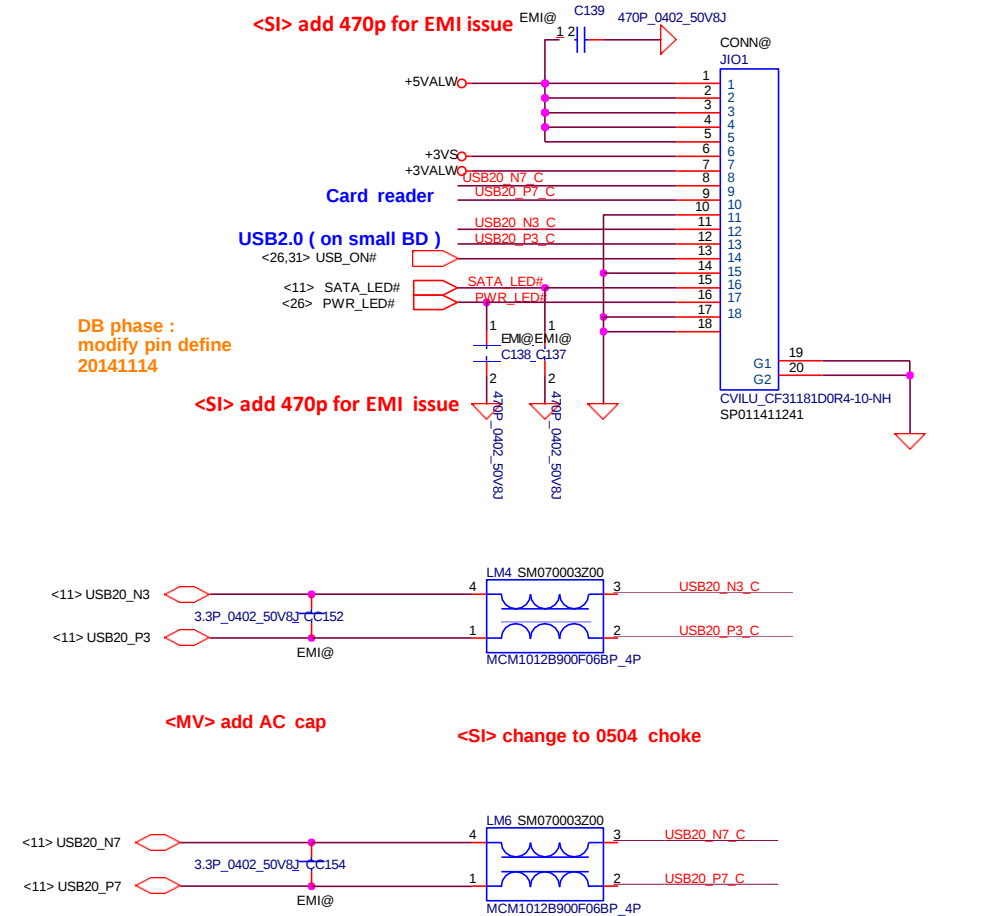


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				USB 3.0/2.0 conn		
				Size Document Number	Rev	
				B	v0.2	
				Date:	Wednesday, May 11, 2016	Sheet 31 of 60

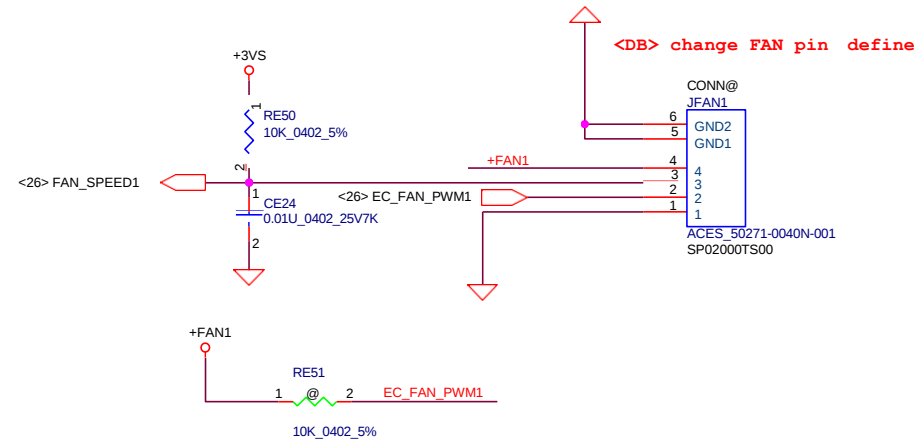
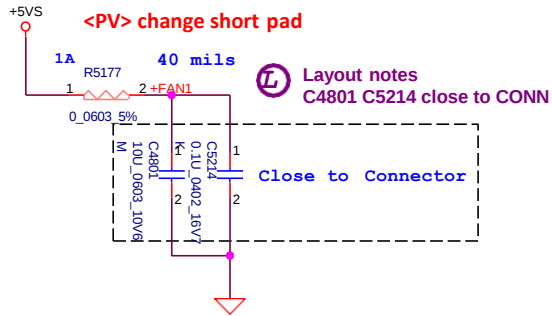
Power Button Connector



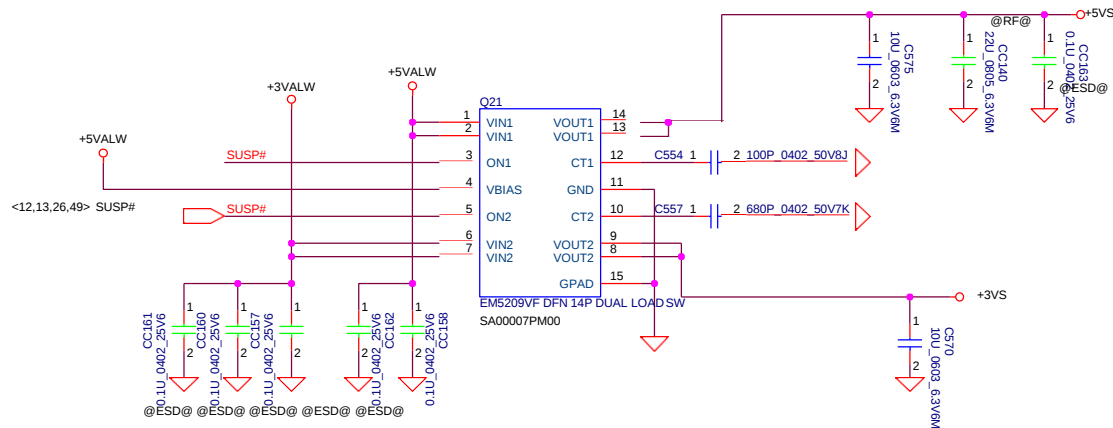
IO BD Connector (USB2.0,Card reader,HDD & PWR LED)



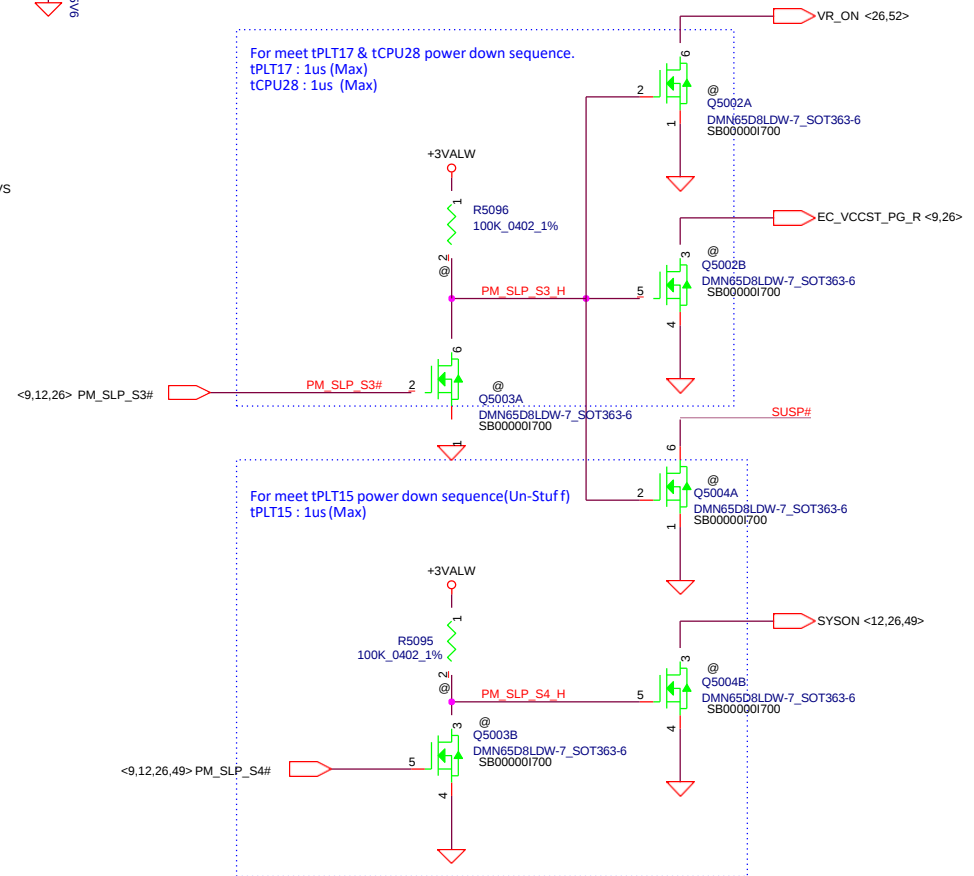
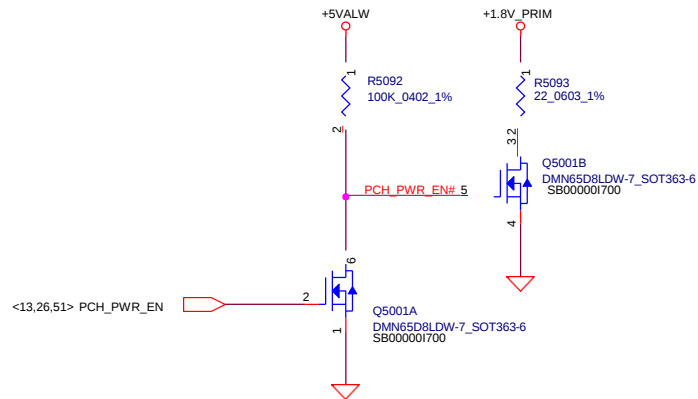
Security Classification	Compal Secret Data				Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	IO CON	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Size Document Number	Rev
					B LA-D707P	v0.2
					Date: Wednesday, May 11, 2016	Sheet 33 of 60



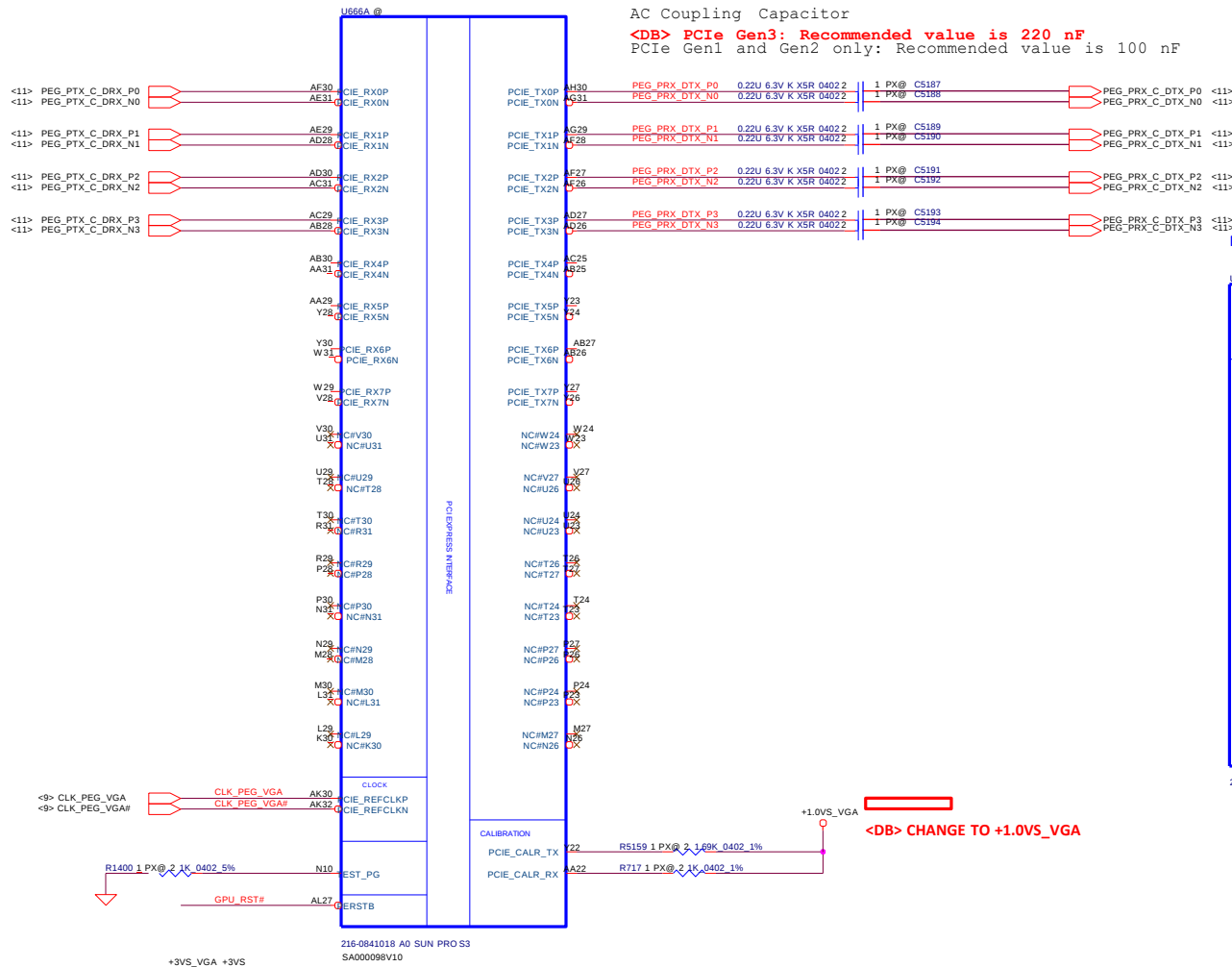
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					Date: Wednesday, May 11, 2016	Sheet 34 of 60	



For +1.8V_PRIM Discharge

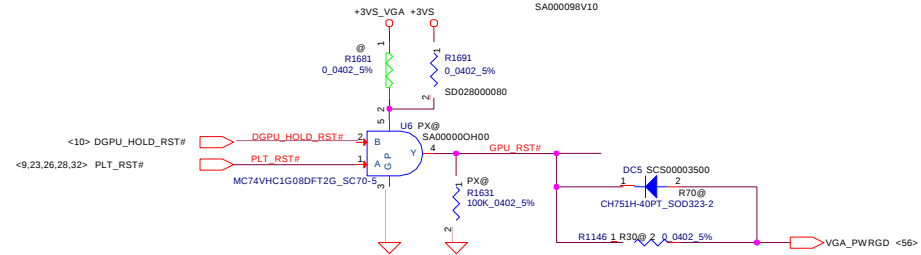
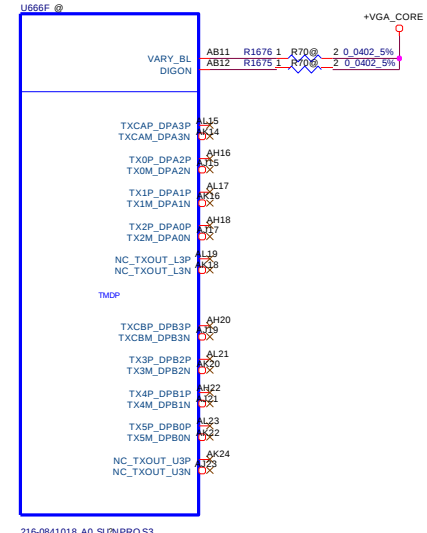


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/10/09	Deciphered Date	2015/12/31	Title	
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				Size/Document Number	Rev
				Custom LA-D707P	v0.2
				Date: Wednesday, May 11, 2016	Sheet 35 of 60

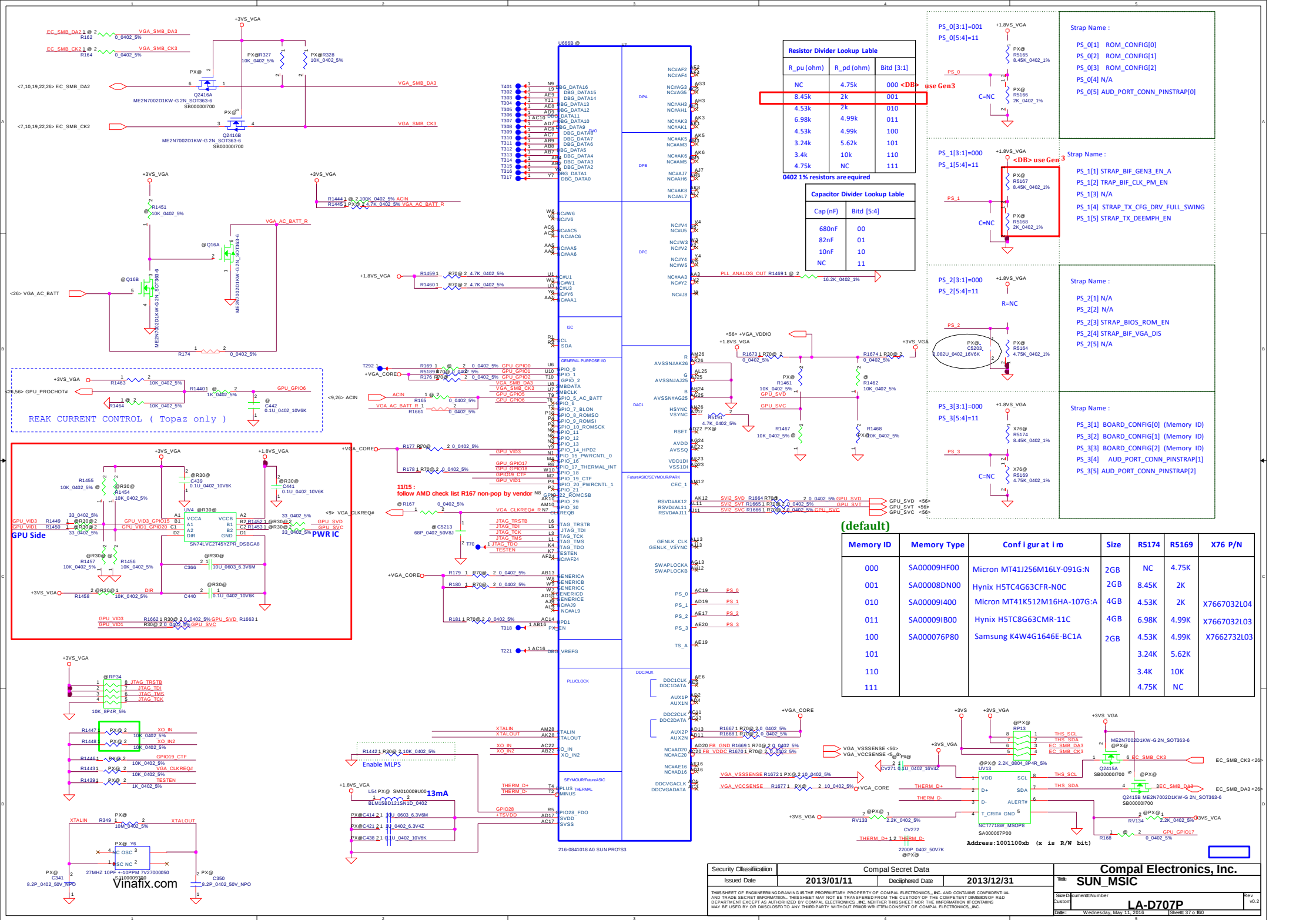


AC Coupling Capacitor
<DB> PCIe Gen3: Recommended value is 220 nF
PCIe Gen1 and Gen2 only: Recommended value is 100 nF

No Use GPU Display Port output



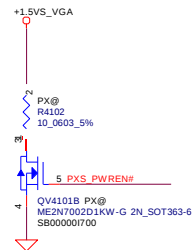
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/01/11	Deciphered Date	2013/12/31	Title	SUN PCIe/DP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size/Document Number	Rev
				Custom	v0.2
				Date	Wednesday, May 11, 2016
				Sheet	36 of 60



+1.5VS to +1.5VS_VGA (2.096A)

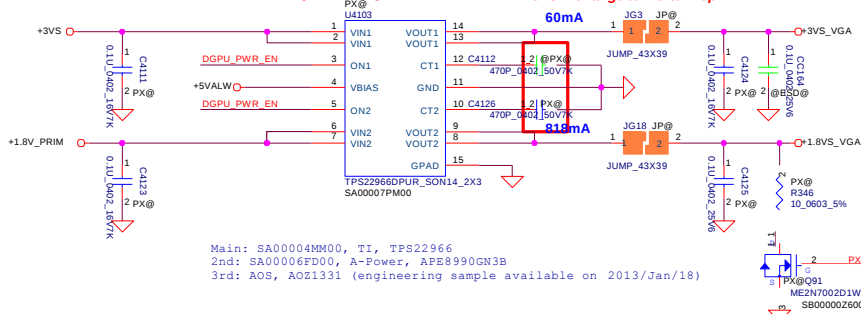


Delete +1.5VS to +1.5VS_VGA power switch



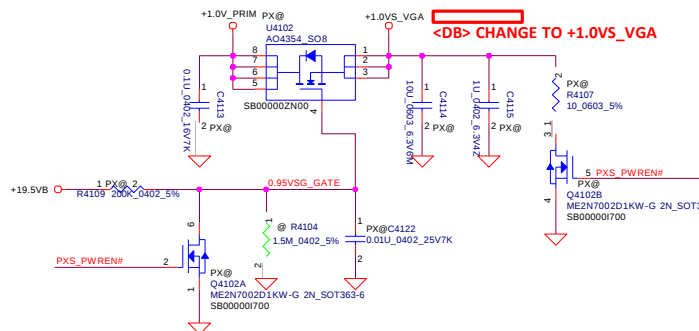
+3VS to +3VS_VGA (25mA)

+1.8V_PRIM to +1.8VS_VGA (311mA)



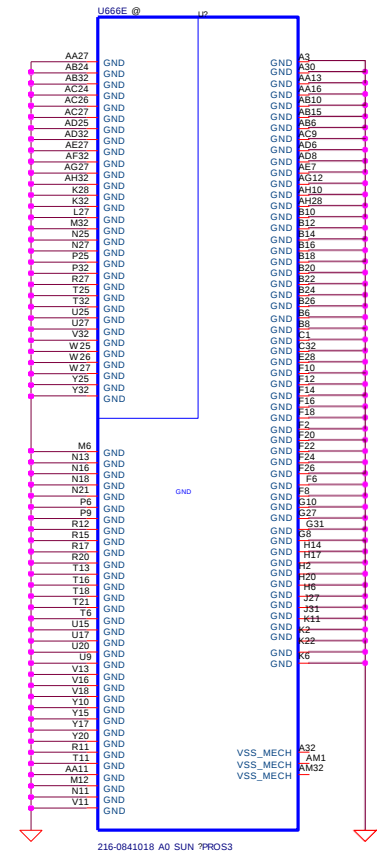
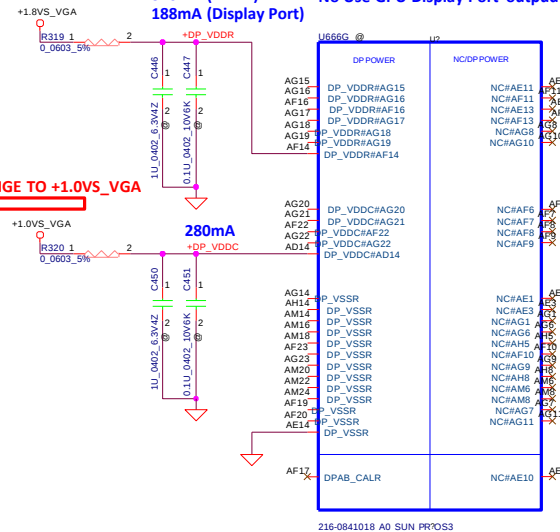
Main: SA00004MM00, TI, TPS22966
2nd: SA00006FD00, A-Power, APE8990GN3B
3rd: AOS, AOZ1331 (engineering sample available on 2013/Jan/18)

+1.0V_PRIM to +1.0VS_VGA (4.016A)



370mA (HDMI) 188mA (Display Port) No Use GPU Display Port output

<DB> CHANGE TO +1.0VS_VGA

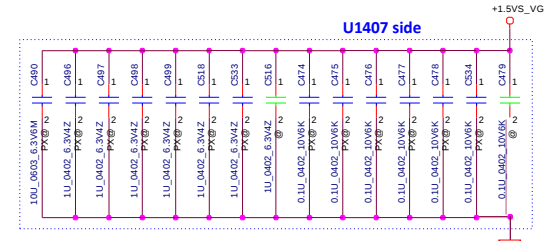
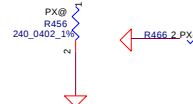
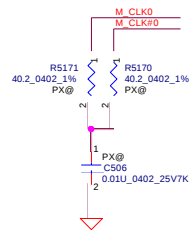


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/01/11	Deciphered Date	2013/12/31	Title	SUN Power/GND
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				LA-D707P	v0.2
				Date	Wednesday, May 11, 2016
				Sheet	38 of 60

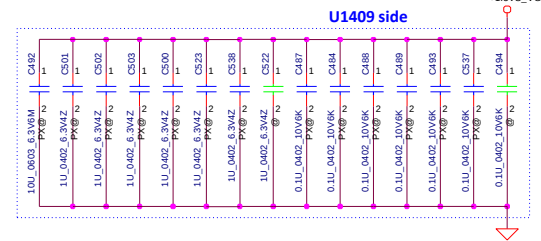
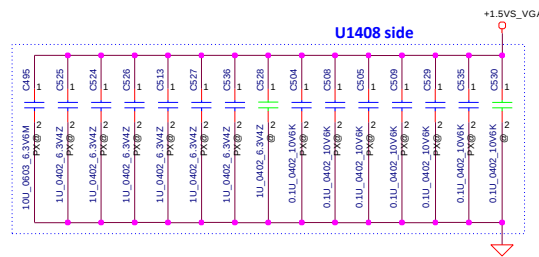


Size Document Number	Rev
Custom	v0.2
LA-D707P	
Date: Wednesday, May 11, 2016	Sheet 40 of 60

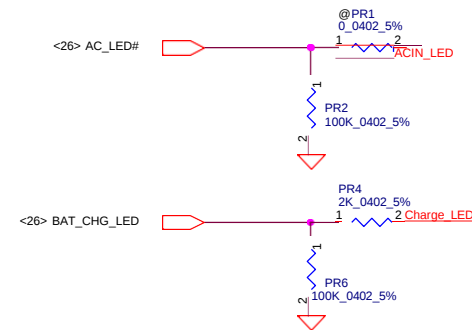
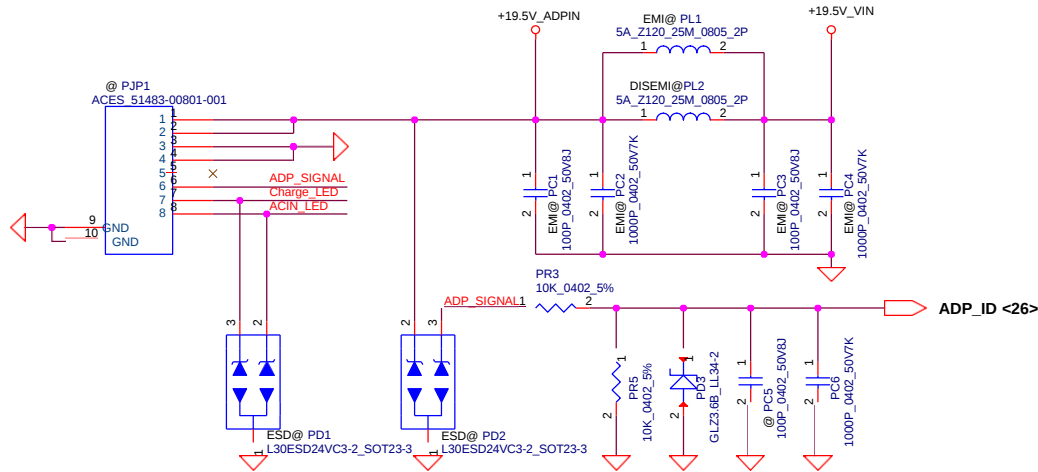
<40,42> M_DA[63..0]		M_DA[63..0]
<40,42> M_MA[15..0]		M_MA[15..0]
<40,42> M_DQM[7..0]		M_DQM[7..0]
<40,42> M_DQS[7..0]		M_DQS[7..0]
<40,42> M_DQS#[7..0]		M_DQS#[7..0]



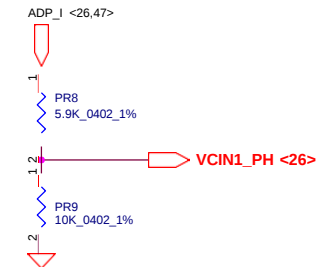
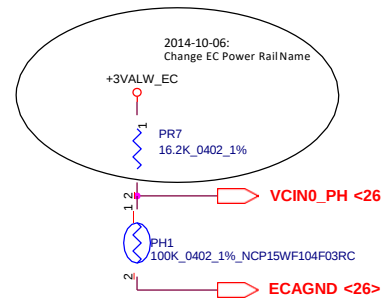
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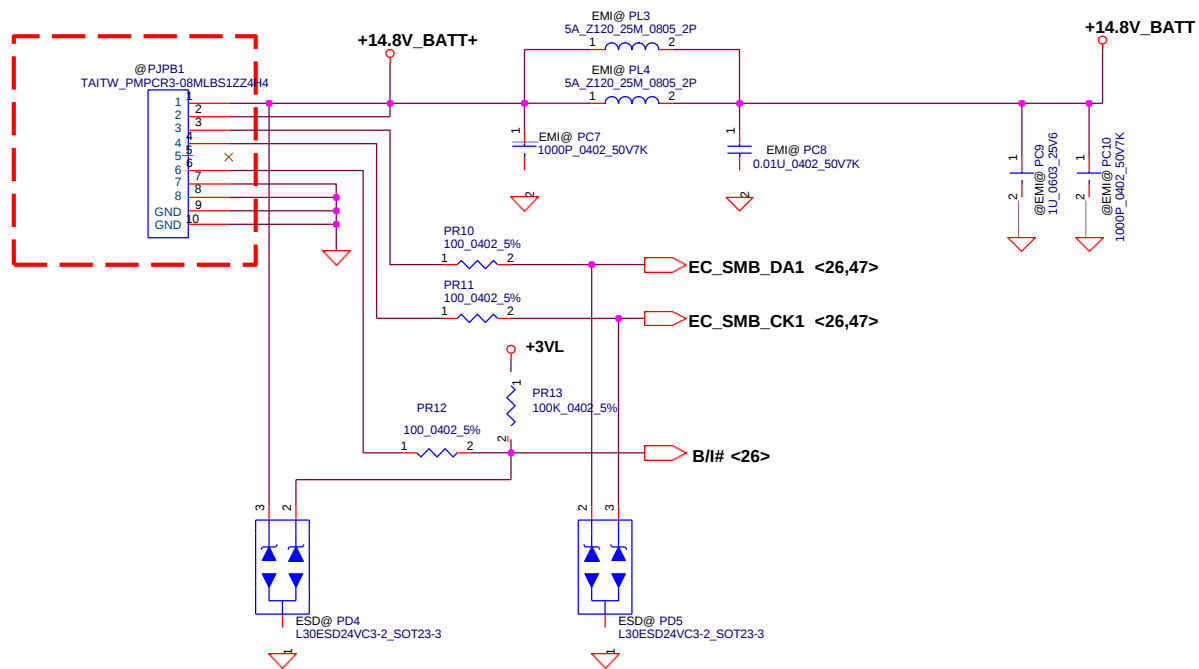


ADP_ID			
Adapter Type		Voltage Range (Dec)	Voltage Range (Hex)
None	Normal Adapter	<0.211V	< 10
	Air-Line Apdater	<0.334V	< 1A
40W	Normal Adapter	>=0.211V ;<0.349V	>= 10 < 1A
45W	Normal Adapter	>=0.349 ;<0.442	>= 1A < 20
65W	Normal Adapter	>=0.442V ;<0.549V	>=20 <2A
	Air-Line Apdater	>=0.334V ;<0.425V	>= 1A < 21
90W	Normal Adapter	>=0.549V ;<0.710V	>= 2A < 36
	Air-Line Apdater	>=0.425 ;<1.391V	>= 21 < 6A
120W	Normal Adapter	>=0.710V ;<1.391V	>= 36 < 6A
ID is shorted to VIN		>=1.391V with Normal and Air-Line	>= 6A



	Initail	Recovery
OTP	92 C	56 C

	Initail	Recovery
45W UMA	0.65V	0.45V
65W DIS	0.95V	0.67V



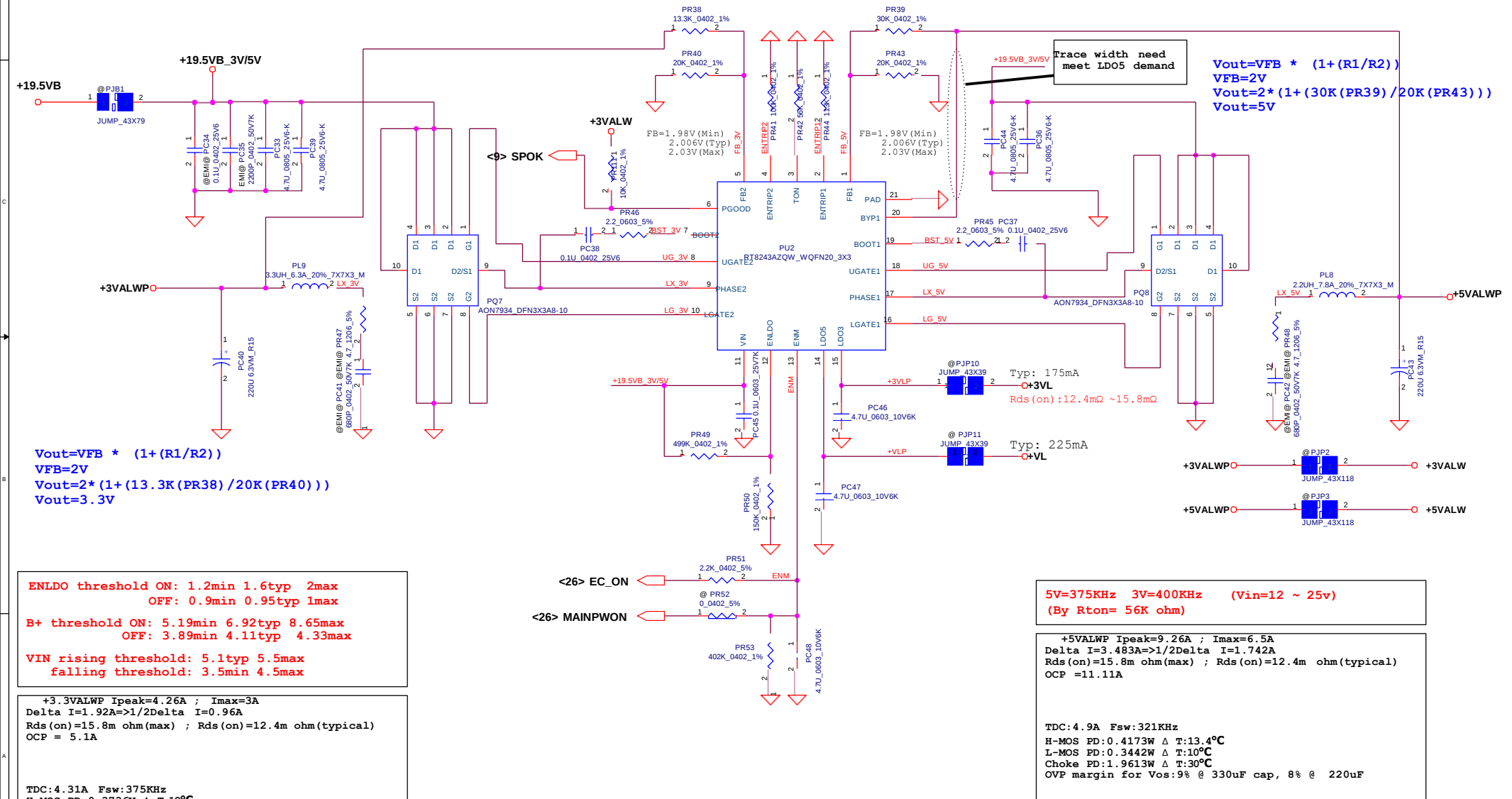
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Module model information

RT8243A_V1.mdd

ENTRIPx adjustment range: 0.5V~3V,
floating or over 4.5V will shutdown channel.

ENLDO (V)	ENM (V)	ENTRIP1 (V)	ENTRIP2 (V)	LDO5	LDO3	+5VALW	+3VALW
Low	Low	X	X	Off	Off	Off	Off
">1.6V" =>High	Low	X	X	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	Off	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	On	On	On	Off	On
">1.6V" =>High	">2.3V" =>High	On	On	On	On	On	On
">1.6V" =>High	">2.3V" =>High	On	Off	On	On	On	Off



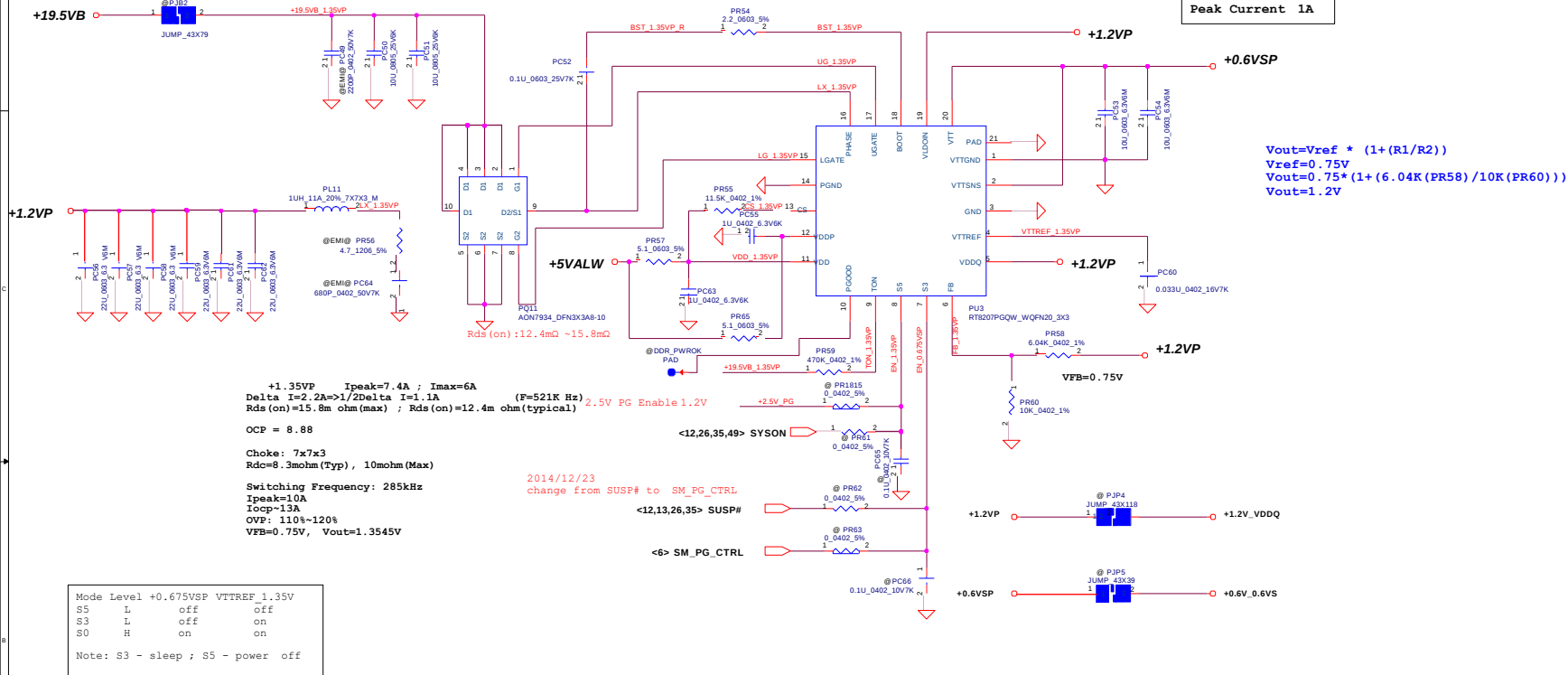
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				Document Number		LA-D707P
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Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Vout +/- 5%
TDC 0.7A
Peak Current 1A

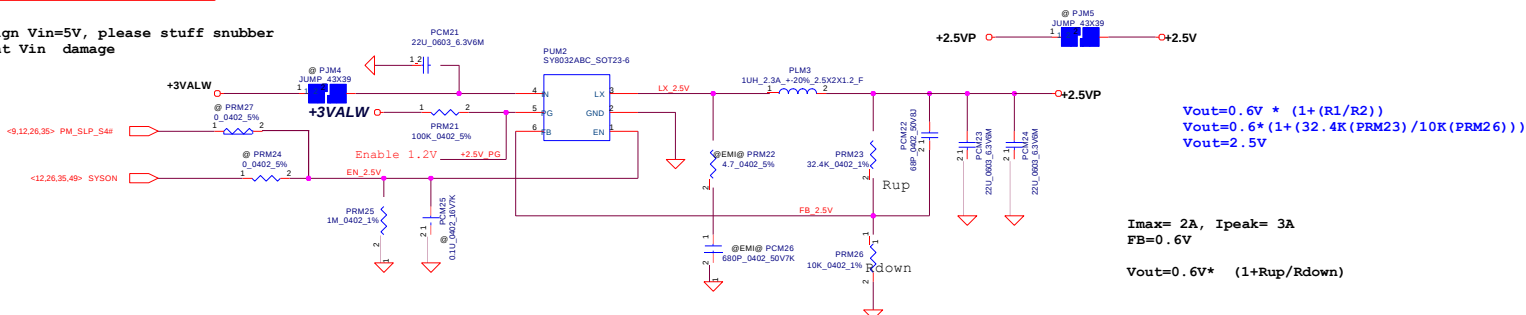


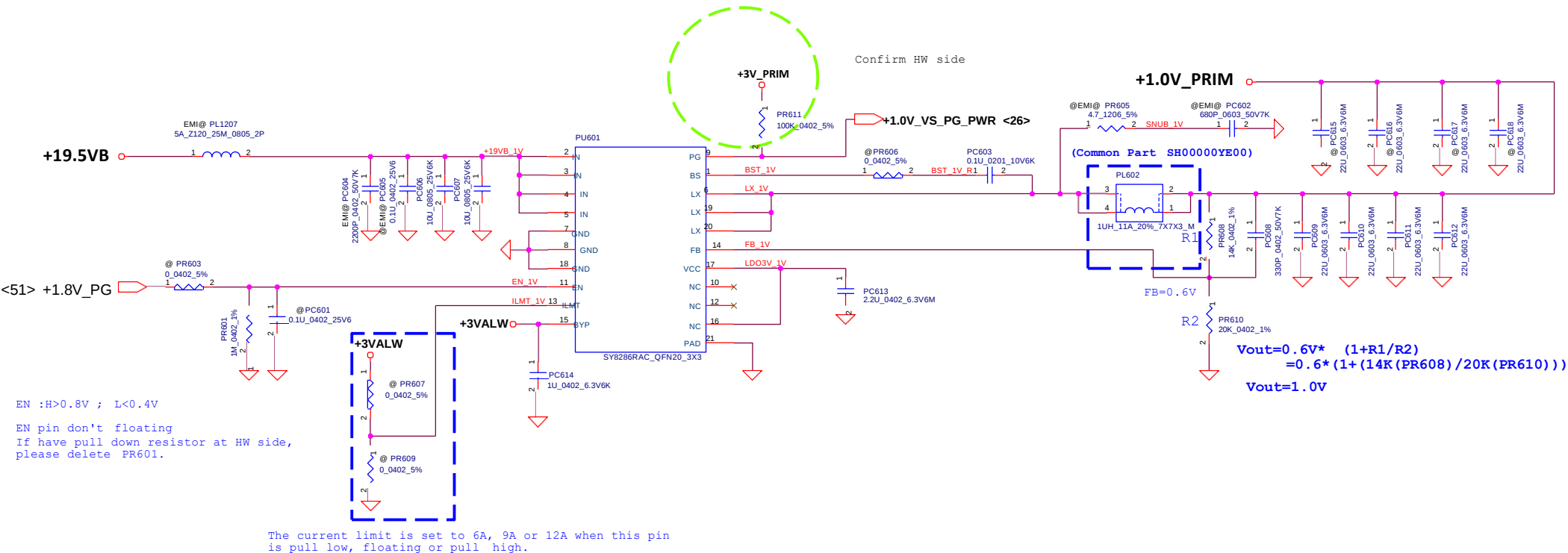
Module model information

SY8032_V2.mdd

Note:

When design Vin=5V, please stuff snubber
to prevent Vin damage

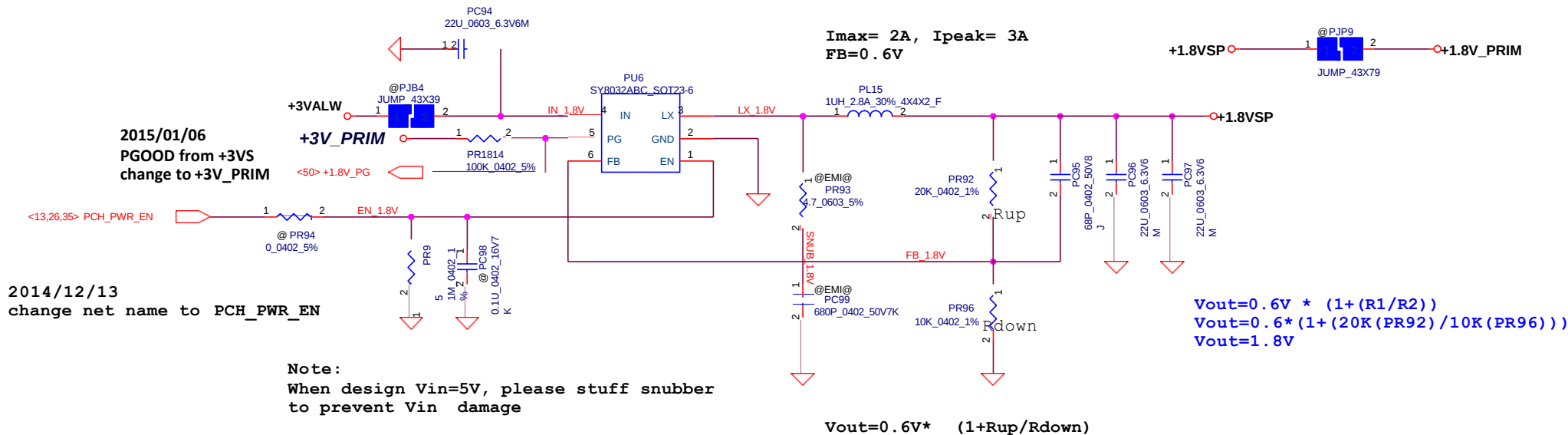




EN :H>0.8V ; L<0.4V
EN pin don't floating
If have pull down resistor at HW side,
please delete PR601.

The current limit is set to 6A, 9A or 12A when this pin
is pull low, floating or pull high.

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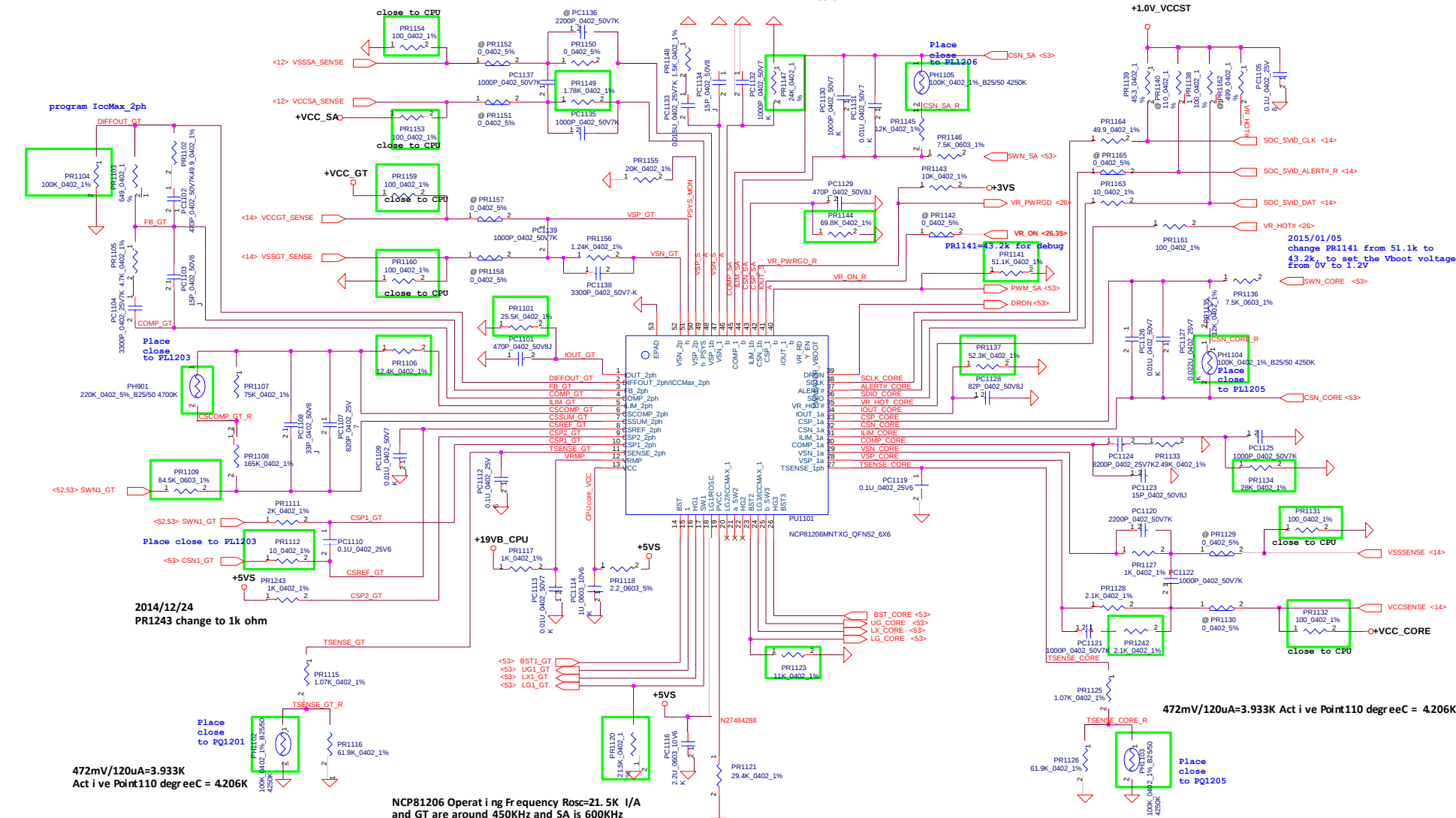
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Date:		Document Number		Rev	
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		60			

Load line= $(PR1108+(PR1107+PH901/(PR1107*PH901)))$ *Iout tital*DCR/PR1109
 U22 Load line@GT= 3.1m
 PR1109 .PR1110@GT=84.5K

RDRPSP(PR1149)= Load line*(PR1146+PH1105+PR1145)/(gm * DCR) /(PH1105+PR1145)
Load line@SA= 10.3m
gm=1mS
PR1149=1.78K

RLIMSP(PR1147)= 1.3V/(gm*(PH1105+PR1145)*IoutLIMIT*DCR/(PR1146+PH1105+PR1145))
OCP@SA= 9.6A
gm=1mS
PR1147=24K

RIOUTSP(PR1144)= 2V/(gm*(PH1105+PR1145)*ICCMAX*DCR/(PR1146+PH1105+PR1146))
IOUTSP@SA= 5A
gm=1mS
PR1144=69.8K



NCP81206 Operating Frequency $R_{osc}=21.5K$ I/A
and GT are around 450KHz and SA is 600KHz

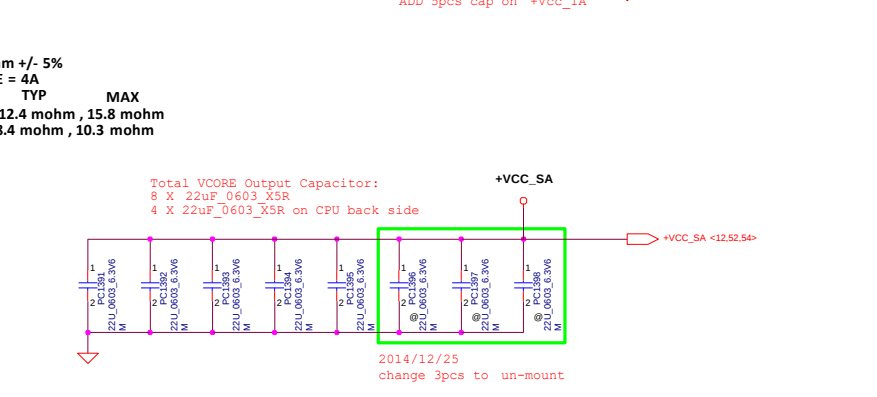
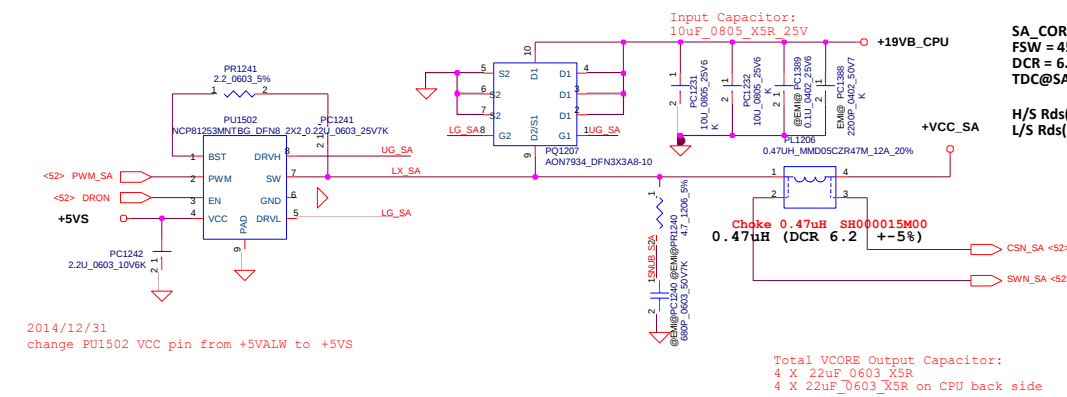
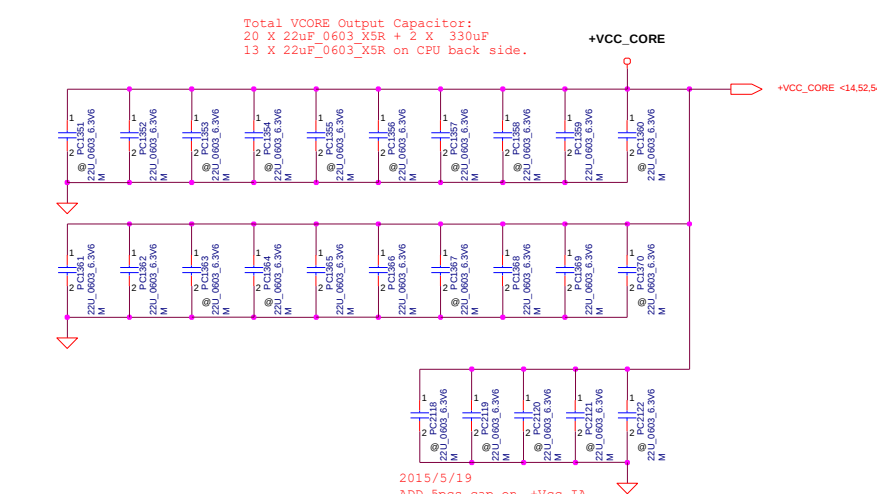
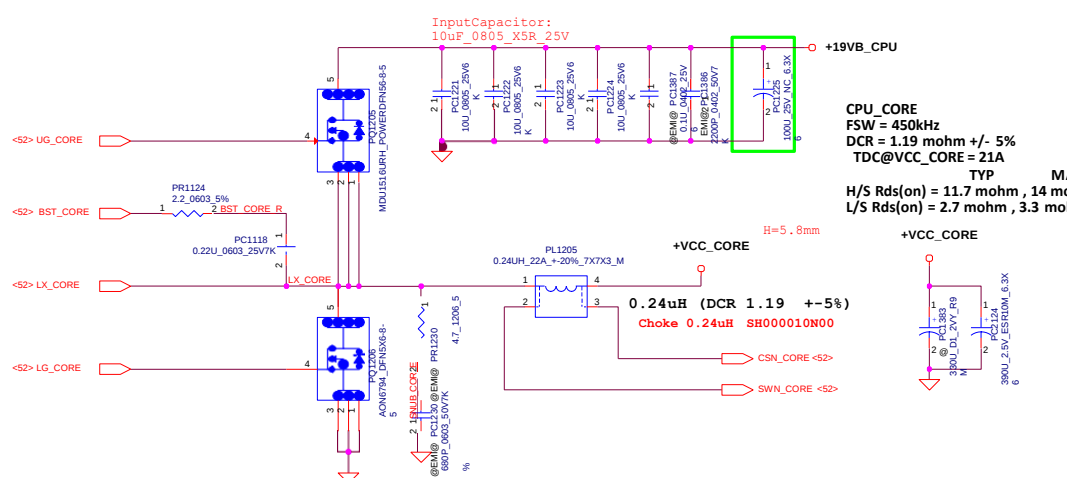
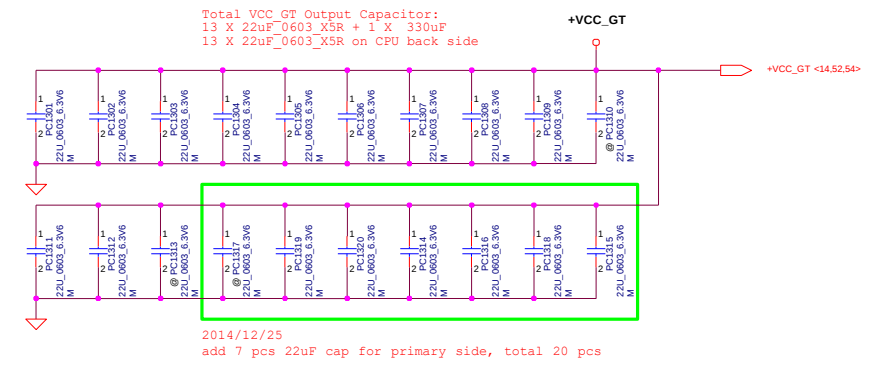
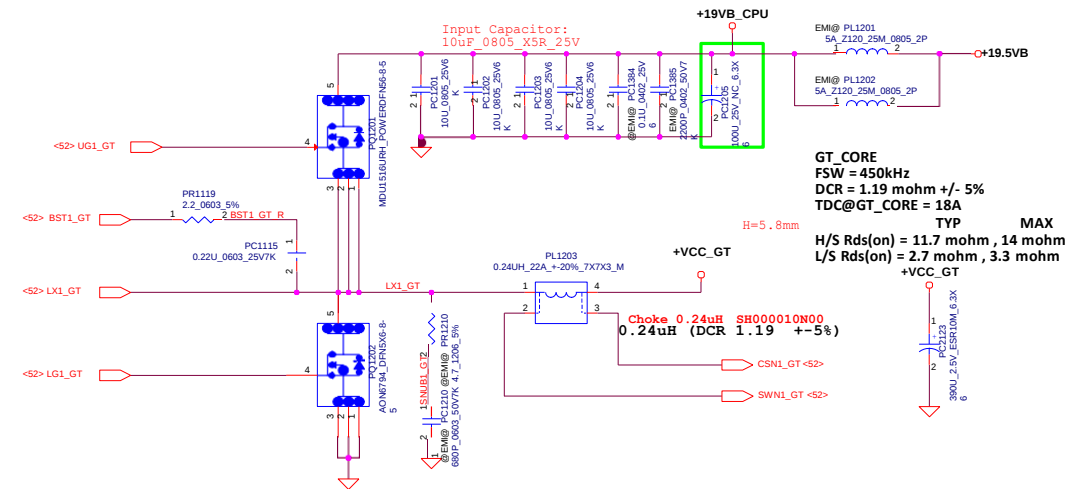
lccMAX@SA= 5A
PR1123= 11K
Refer lccMAX table in datasheet

IccMAX@VCORE= 28A
RlccMAX@VCORE= 24.9K
Refer IccMAX table in datasheet

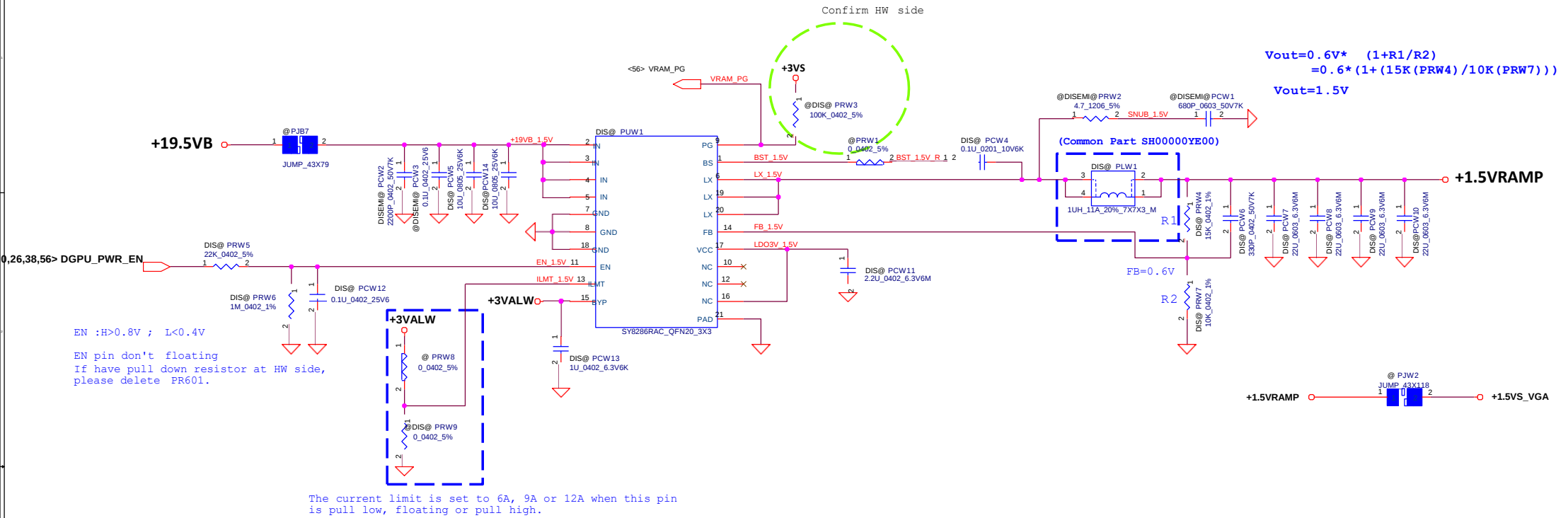
$\text{RDRPSP}(\text{PR1128}) = \text{Load line} * (\text{PR1136} + \text{PH1104} + \text{PR1135}) / (\text{gm} * \text{DCR}) / (\text{PH1104} + \text{PR1135})$
 Load line@VCORE= 2.1m
 gm=1mS
 PR1128=2.1K

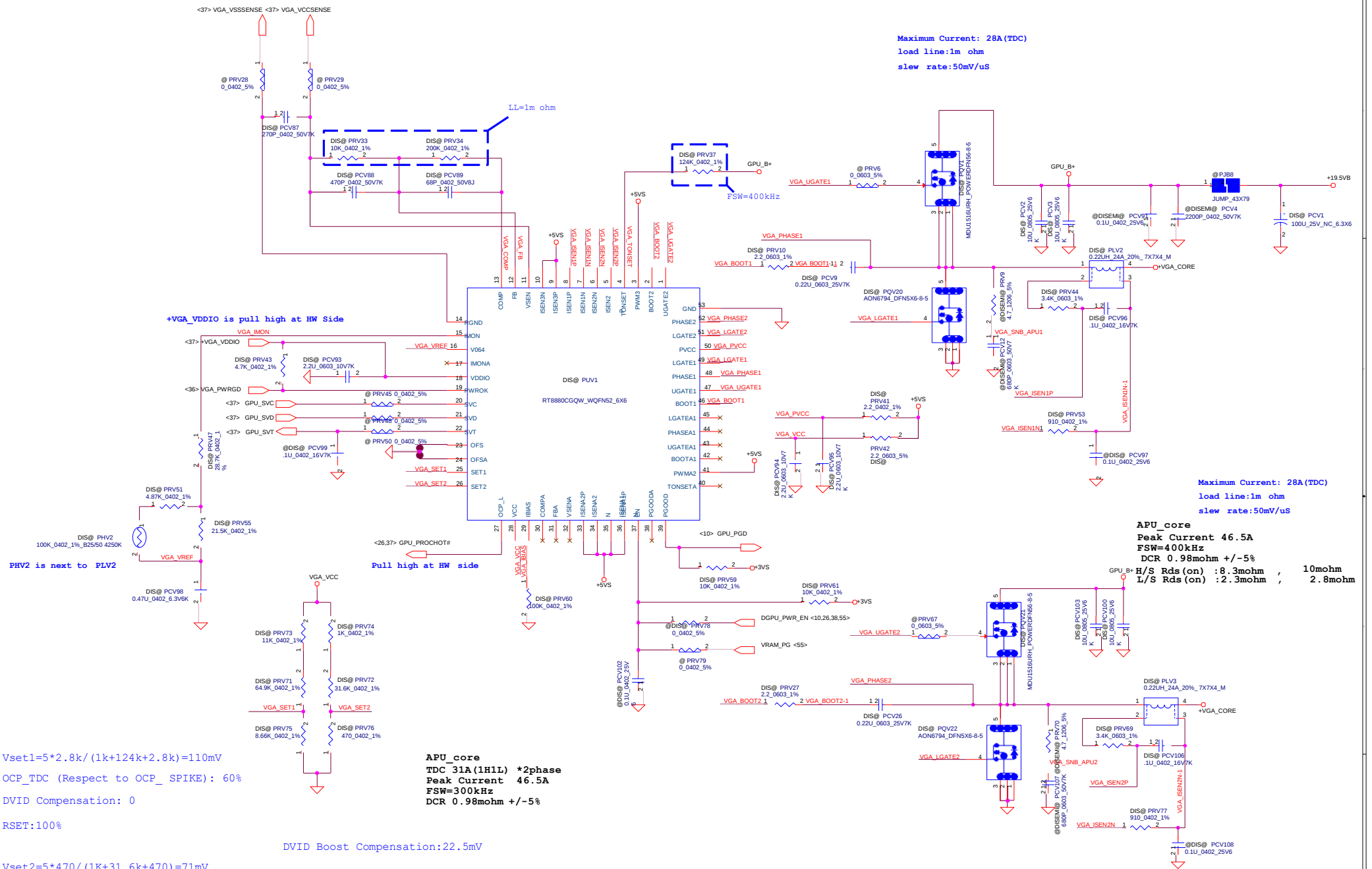
```
RIOUTSP(PR1137)= 2V/(gm*(PH1104+PR1135)*ICCMAX*DCR/(PR1136+PH1104+PR1135))
IOUTSP@VCORE= 28A
gm=1mS
```

PR1137=64.9K
RLIMSP(PR1134)= 1.3V/[gm*(PH1104+PR1135)*IoutLIMIT*DCR/((PR1136+PH1104+PR1135))
OCP@VCORE= 35A
gm=1mS
PR1134=33.2K



2014/12/31
change PUI502 VCC pin from +5VALW to +5VS





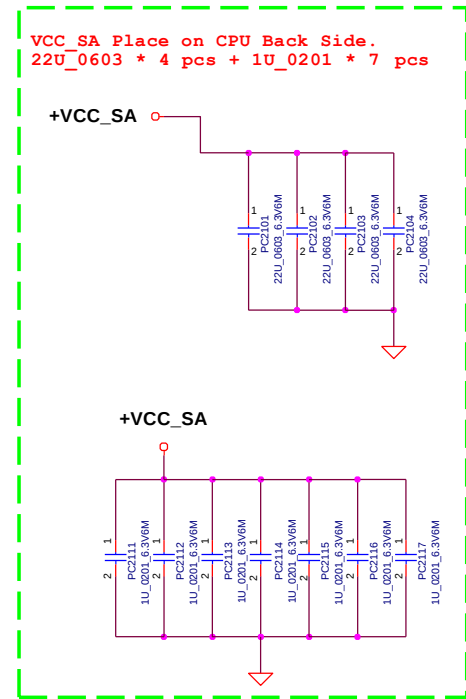
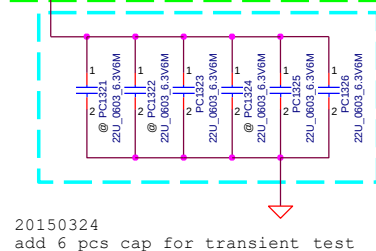
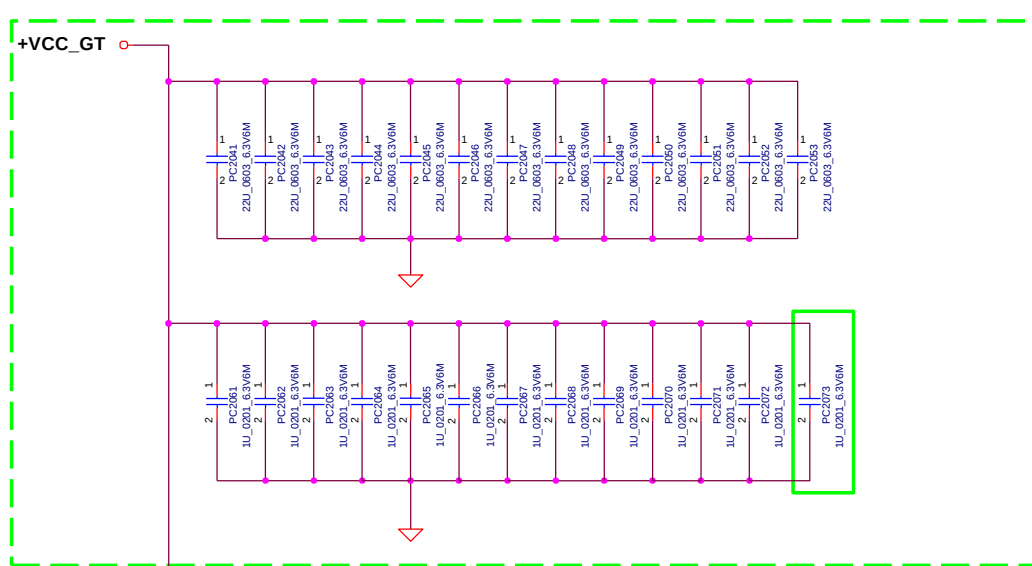
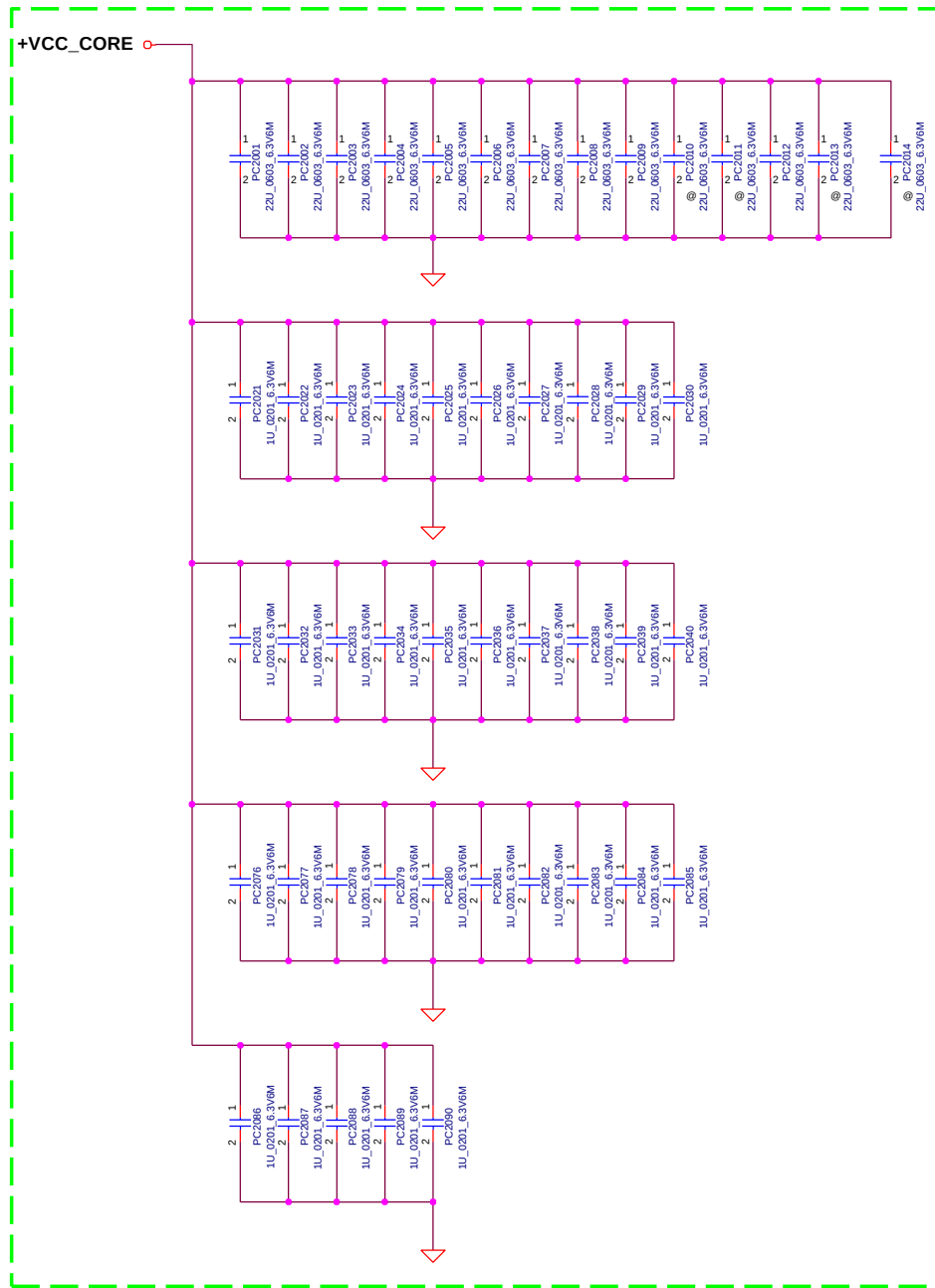
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VCC_CORE Place on CPU Back Side.
22U_0603 * 13 pcs + 1U_0201*35 pcs

VCC_GT Place on CPU Back Side.
22U_0603 * 13 pcs + 1U_0201*12 pcs

2014/12/25
add 1 pcs 1uF cap for back side, total 13 pcs



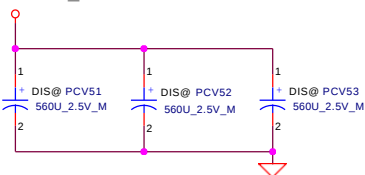
Item	Page	Title	Change Description	Date
1	50,55	Change 0 ohm to short pad	Change PR607,PRV28,PRV29 from 0 ohm to short pad PRW8 from unpop to pop , change PRW8 from 0 ohm to short pad	2016-2-19
2	53,56	High Low Side MOS Matrix request	Change PQ1201,PQ1205,PQV1,PQV21 from SB000003800 to SB00000JZ00(Change to Main source)	2016-2-19
3	54	Add IA_Core Output capacitor	Add IA_Core Output capacitor 0603 22uF(PC2014) for IcdMATE=32A	2016-2-24

Item	Page	Title	Change Description	Date
1	47	ADP_I resistance	Change PR223 from short pad to 0 ohm	2016-4-28
2	52	IOccmax from 29A to 32A	Change PR1121 from 20.5K to 29.4K Change PR1137 from 61.9K to 52.3K Change PR1134 from 33.2K to 28K	2016-4-28
3	53,56	High Low Side MOS Matrix request	Change PQ1201,PQ1205,PQV1,PQV21 from SB00000JZ00 to SB000003800 (Change to 2nd source)	2016-4-28
4	49	Add 2nd source	Change PU3 from RT8207P (SA00007IH00) to G5616B (SA00008PH00)	2016-4-28
5	48	Add 2nd source	Change PU2 from RT8243A(SA00005VH00) to UP1590PQKF (SA00007DS00)	2016-4-28

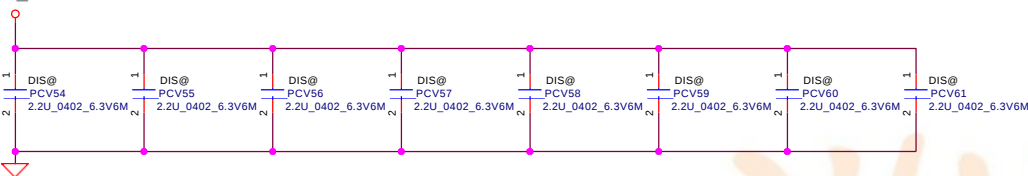
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	52	Change Value	11/06	Power	(Set VR proctot# from 110C to 120C)	Change PR1115 and PR1125 Value 0 ohm to 1.07K ohm	
2	50	Change part number	11/06	Power	Change from 5x5 choke to 7x7 follow Candy design	Change PL602 part number from SH00000Z200 to SH00000YE00	
3	55	Change part number	11/06	Power	Change from 5x5 choke to 7x7 follow Candy design	Change PLW1 part number from SH00000Z200 to SH00000YE00	
4	48	Add Jump	11/18	Power	For easy debug	+3VL and +VL add Jump	
5	55	Add Net	11/18	EE	For VGA CORE sequence and VID error issue	Delete PG pin test point VRAM_PG Add Net VRAM_PG	
6	56	pop to unpop unpop to pop	11/18	EE	For VGA CORE sequence and VID error issue	PRV61 from unpop to pop PRV78 and PCV102 from pop to unpop	
7	56	Add Net and R	11/18	EE	For VGA CORE sequence and VID error issue	Add Net VRAM_PG Add PRV79	
8	47	Change jump to ISN choke	11/24	EMI	EMI ISN issue	Delete jump PJB9 Add ISN choke PL201	
9	48	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL7	
10	49	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL10	
11	50	Change jump to Bead	11/24	EMI	EMI power noise issue	Delete jump PJB3 Add Bead PL1207	
12	53	Change jump to Bead	11/24	EMI	EMI power noise issue	Delete jump PJB5 Add Bead PL1201 PL1202	
13	55	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL1208	
14	56	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL1209 and PL1210	
15	55	Change R Value Change C unpop to pop	11/24	EE	HW f i net une VRA Mpowersequence	Change PRW5 value from 0 ohm to 22K ohm Change PCW12 from unpop to pop (VGA sequence)	
16	53	Change Common part	11/6	Power	(Change to Common part)	Change PC1331 PC1383 PC1390 from SGA20331E10 to SGA00009S00	

Item	Page	Title	Change Description	Date
1	56	Modify VGA_CORE OCP	1.Change PRV73 Value 1K ohm to 11K ohm 2.Change PRV71 Value 124K ohm to 64.9K ohm 3.Change PRV75 Value 2.5K ohm to 8.66K ohm	2015-12-12
2	47	space saving	Change PC221 0603 to 0402 size	2015-12-12
3	47,49, 50,51, 52,56	Change 0 ohm to short pad	Change PR63, PR94, PR215, PR603, PR1129, PR1130, PR1142, PR115 1, PR1152, PR1157, PR1158, PR1165, PR1815, PRM27, PRV45 , PRV48, PRV50, PRV79, PRV6, PRV67 from 0 ohm to short pad	2016-1-4
4	48,49, 55,56	Delete Jump or Bead(Co- lay)	Delete Co-Lay Bead PL7, PL10, PL1208, PL1209, PL1210	2016-1-7
5	53	Delete WOC_GT, WOC_CORE Co-Lay caps	Delete Location PC1331 Footprint, PC2123 from unpop to pop Delete Location PC1390 Footprint, PC2124 from unpop to pop	2015-12-12
6	53,56	High Low Side MOS Matrix request	Change PQ1201, PQ1205, PQV1, PQV21 from SB00000JZ00 to SB00000S900	2015-12-12
7	52,53, 54	CPU transient request	Change PC1353, PC1363, PC1355, PC1356, PC1357, PC1354, PC1364 , PC1358, PC1351, PC1370, PC1360, PC2010, PC2013, PC201 1, PC1367 from pop to unpop Change PC1107 from 1000P to 820P PC1108 from 390P to 33P, PC1108 from unpop to pop PC1104 from 2200P to 3300P PR1103 from 1K to 649	2015-12-12
8	50	1V OVP issue (HW Low switch second source issue)	Delete jump PJ601 and add output MLOC PC615, PC616, PC617, PC618 PR607 from unpop to pop	2016-1-7

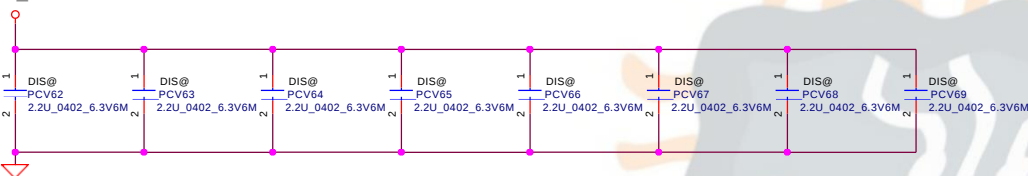
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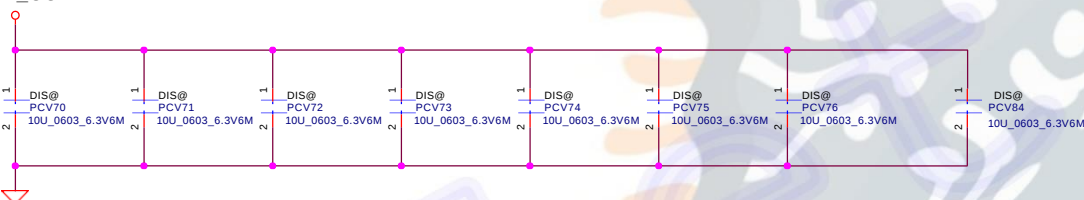
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+VGA_CORE

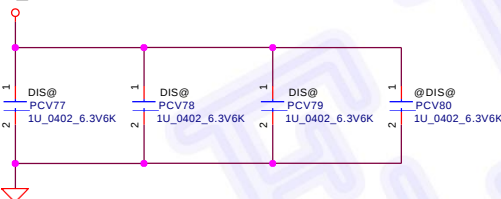


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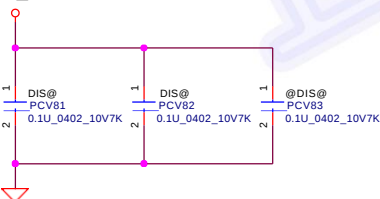


560u X 3
2.2u X 16
10u X 8
1u X 3
0.1u X 2

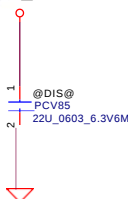
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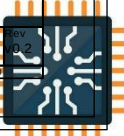
+VGA_CORE



+VGA_CORE



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BOM control

Plat f orm	Silego P/N	Compal PN	25MHz(A)	32.768KHz	24MHz(B)	27MHz	8MHz	Remark
Intel ULT UMA	SLG3NB3455VTR	SA00008IQ00	1	1	1	X	X	GCLKUMA@
Intel ULT Dis	SLG3NB3456VTR	SA00008J800	1	1	1	1	X	GCLKPX@

Base on A32 32.768KHz use 10ppm, G-CLK 25MHz X" TAL use 10ppm.